ABSTRACT

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Michael A. Holloway, Doctor of Philosophy, 2010

Directed By: Professor & Chair, Patrick G. O'Shea, Department of Electrical and Computer Engineering

The intentional use of high power microwave (HPM) signals to disrupt microelectronic systems is a substantial threat to vital infrastructure. Conventional methods to assess HPM threats involve empirical testing of electronic equipment, which provides no insight into fundamental mechanisms of HPM induced upset. The work presented in this dissertation is part of a broad effort to develop more effective

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14. ABSTRACT

The intentional use of high power microwave (HPM) signals to disrupt microelectronic systems is a substantial threat to vital infrastructure. Conventional methods to assess HPM threats involve empirical testing of electronic equipment which provides no insight into fundamental mechanisms of HPM induced upset. The work presented in this dissertation is part of a broad effort to develop more effective means for HPM threat assessment. Comprehensive experimental evaluation of CMOS digital electronics was performed to provide critical information of the elementary mechanisms that govern the dynamics of HPM effects. Results show that electrostatic discharge (ESD) protection devices play a significant role in the behavior of circuits irradiated by HPM pulses. The PN junctions of the ESD protection devices distort HPM waveforms producing DC voltages at the input of the core logic elements, which produces output bit errors and abnormal circuit power dissipation. The dynamic capacitance of these devices combines with linear parasitic elements to create resonant structures that produce nonlinear circuit dynamics such as spurious oscillations. The insight into the fundamental mechanisms this research has revealed will contribute substantially to the broader effort aimed at identifying and mitigating susceptibilities in critical systems. Also presented in this work is a modeling technique based on scalable analytical circuit models that accounts for the non-quasistatic behavior of the ESD protection PN junctions. The results of circuit simulations employing these device models are in excellent agreement with experimental measurements, and are capable of predicting the threshold of effect for HPM driven non-linear circuit dynamics. For the first time, a deterministic method of evaluating HPM effects based on physical, scalable device parameters has been demonstrated. The modeling presented in this dissertation can be easily integrated into design cycles and will greatly aid the development of electronic systems with improved HPM immunity.

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CHARACTERIZATION AND MODELING OF HIGH POWER MICROWAVE EFFECTS IN CMOS MICROELECTRONICS

By

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Dedication

To my parents Theodore B. Holloway Jr. and Shirley L. Holloway for all of their love, support, and sacrifices.

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It is difficult to find the words of gratitude to adequately express my profound appreciation to so many people who have mentored, encouraged, and inspired me during my time as a student in IREAP. My journey began when I met Professor Patrick O'Shea in spring of 2002. I was a student in his basic circuit theory class when he offered me a job to work in his lab as an undergraduate. From that point on he has been a constant mentor, advisor, and example. He has encouraged and supported me at every step in my journey. I am forever grateful for all Professor O'Shea has done for me. Working with Dr. John Rodgers over the past two years has truly been a privilege. Dr. Rodger's is a brilliant experimentalist who is dedicated to his students. I will cherish the opportunity I had to work with him and always appreciate the fact that I had a research advisor who also liked to talk football. I would like to thank Dr. Zeynep Dilli who has gone out of her way to assist me many times. I would also like to offer a special thanks to Dr. Neil Goldsman who generously offered advice both academic and personal, and who gave me the opportunity to work with him on some very exciting projects outside of my doctoral research. I am also very grateful to have worked Dr. Ralph Fiorito and Dr. Anatoly Shkvarunets who mentored me for my Masters research. Many more names and many more stories could fill endless pages of this acknowledgement. So I would like to thank all of the many people of IREAP who I have ever had the great privilege to work with, to call colleagues, and most importantly, to call friends. I would also like to thank the Air Force Office of Scientific Research for their support of this work.

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Chapter 1 : Introduction

1.1 Motivation

Over the past few decades, technology has advanced at an astonishing pace. Equally astonishing is how quickly human civilization has adopted and assimilated new technologies into every facet of life. Many clever inventions begin as a convenience or luxury but quickly become a dependency as their practicality often relieves the drudgery of cumbersome and time consuming tasks. Among the greatest inventions of the 20th Century and perhaps even in all of human history is the integrated circuit. Microelectronic technology has become ubiquitous; so much so that daily life depends on microelectronic systems. The emergence of interconnected systems enabled by the growth of the internet has furthered our reliance on microelectronic systems. Much of our financial system exists as digital data stored in vast networks of computer systems accessible completely through the internet. Commercial transactions are often completed without the use of paper currency via the internet or wireless devices. Microelectronic systems have also greatly enhanced medical technology and improved overall health care considerably compared to only a few decades ago. Vital civil infrastructure such as traffic control systems, public transportation, automobiles, aircraft, and ships all rely on a myriad of microelectronic control and communication systems.

With the unending proliferation of technology comes an increased need to protect vital systems from potentially catastrophic disruptions. Generically, this is referred to as *cyber security*. Most of the global conversation regarding cyber

security deals with software driven attacks and network breaches. However, an emerging concern, critical to cyber security, is the protection of the physical layer. An attack on the physical layer refers to a directed attack on the microelectronic devices themselves. An example of such a physical layer threat that is gaining considerable attention in both military and civilian sectors is the ability of microwave radiation to disrupt the proper function of microelectronic systems. Microwave energy is transmitted by many sources such as radar, cell phone towers, Wi-Fi transmitters, satellite communications, or even portable electronic devices.

The phenomenon of errant microwave signals interfering with the operation of electronics systems is not an entirely new concern. Anyone traveling by commercial jet has experienced the request to refrain from using portable electronic devices during the critical moments of takeoff and landing. Disruption from electromagnetic interference (EMI) generated by electronic equipment and wireless systems has been studied for some time. In the United States, electronic systems must meet electromagnetic compatibility standards (EMC) to ensure that equipment is able to function reliably in its electromagnetic environment without itself introducing intolerable electromagnetic disturbances [1]. Also, aircraft must have adequate shielding to protect instrumentation from high power sources such as radar [2].

The greater and more substantial threat to infrastructure and equipment is the intentional emission of microwave energy to disrupt or damage microelectronic systems. A focused attack from a high powered microwave (HPM) source can disrupt or destroy critical systems with potentially lethal consequences. The concern about such a scenario occurring has increased considerably over the past two decades

[3-14]. The threat of terrorism has prompted the evaluation of the susceptibility of electronic systems to the HPM threat in the US and many European countries. Many systems remain unprotected, and EMC standards set by governing authorities regulate electric fields produced by low-level of microwave emissions. The vulnerability of electronic systems to HPM is a glaring Achilles heel to vital civil infrastructure that must be addressed.

1.2 Fundamental Description of HPM Effects

The term "*HPM effects*" as used throughout the body of this work refers to the specific behavior or physical effects in microelectronic systems that occur as a result of intentional focusing of high power microwave energy onto the system. HPM interaction with microelectronics systems is a very complex phenomenon when one considers all the elements involved in a typical HPM effects scenario. It is comprised of several fundamental stages, as depicted in Figure 1. A source of directed energy emits HPM radiation, which penetrates enclosures and excites EM modes within the enclosure. Circuit board traces and wires act as antennas that couple EM energy into microelectronic devices. The devices respond to the HPM excitation, producing effects that will potentially trigger system upset or cause physical damage.

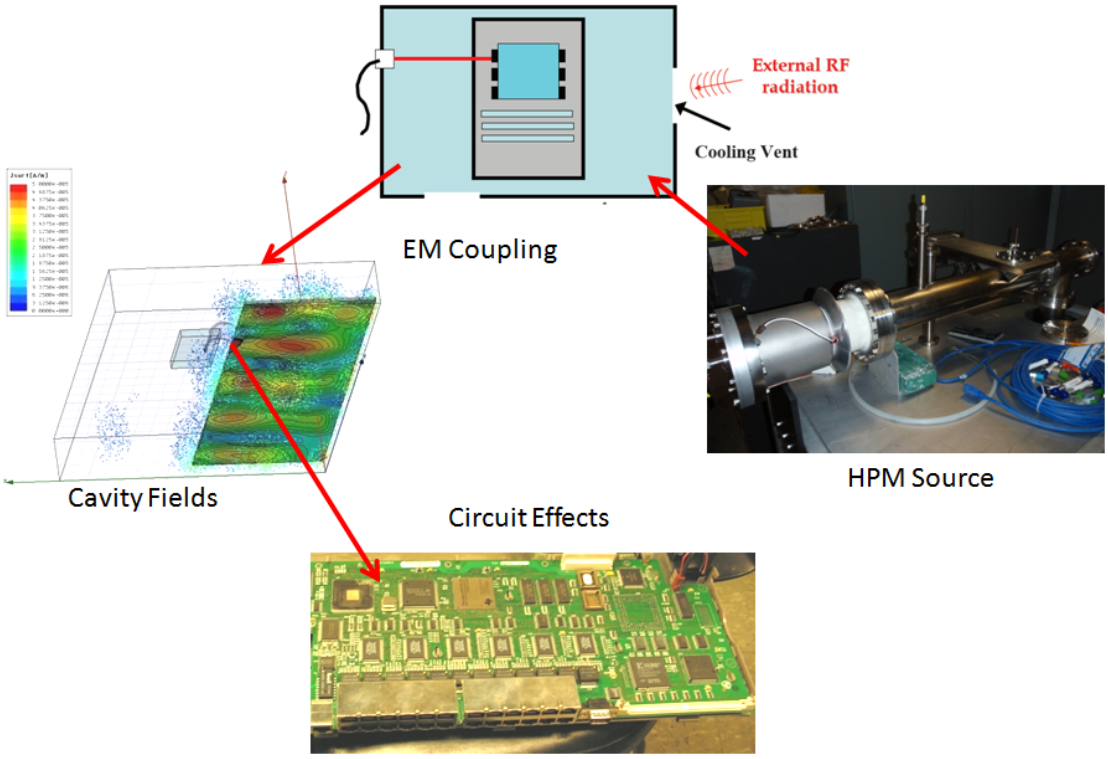

Figure 1.1: Primary elements of typical HPM effects scenarios

1.2.1 HPM Sources

A survey of the literature will reveal a somewhat ambiguous classification of what qualifies as an HPM source [6, 11, 15, 16]. In general an HPM source is classified as one that is capable of producing at least 100 MW of peak RF power in the frequency range of 1 MHz to 100 GHz, with pulse durations that range from tens of nanoseconds to a few microseconds [15, 17, 18]. Examples of HPM sources include klystrons, magnetrons, and gyrotrons.

1.2.2 EM Coupling and Cavity Effects

HPM will couple to microelectronic systems in many ways. Any system that communicates with the outside world will have ingress paths that potentially harmful electromagnetic energy can penetrate. Electromagnetic coupling to a system is

typically considered in two categories. "Front door" is defined as the HPM coupling to systems through ports intended to transmit signals for communication with other systems[4]. Wireless systems with antennas such as Wi-Fi, cells phones, and blue tooth are good examples of systems with front door vulnerability. Protecting systems from front door coupling presents a particularly difficult challenge. Any attempt to attenuate or filter unwanted signals will also adversely affect the reception and processing of normal signals. Also, receiver systems typically have low noise amplifiers, which could unintentionally amplify harmful signals [13].

"Back door" coupling is defined as electromagnetic coupling to wires, power lines, circuit traces, or any part of the system not specifically designed to transmit or receive RF signals [4]. Back door coupling creates voltages on traces and wires that superimpose with normal signals and enter device terminals. While circuit traces and wires are not designed specifically to transmit and receive signals, they introduce parasitic resonances in systems that reduce the level of RF power required to stimulate HPM effects [4].

Cavity fields are another important aspect of HPM effects. HPM will penetrate enclosures such as computer cases and excite field distributions according to the resonant modes of the structure. Predicting these field distributions deterministically is difficult due to the complexity of the EM boundary conditions that are typical of even the most basic electronic enclosures. Often times the dimensions of the enclosures and the corresponding EM boundaries are many times greater than the wavelength of the HPM radiation. Thus, structures support numerous modes that are typically closely spaced in frequency [19]. Further complicating the

analysis of EM fields is the fact that the EM boundaries are rarely static. Small changes due to motion, vibration, or temperature may substantially alter the field distribution.

1.2.3 Circuit and Device Effects

As technology advances towards smaller faster devices, the potential of microwave energy to disrupt electronic systems may increase [12, 20]. Smaller electronic devices require less charge to switch states and have reduced noise margins [20]. Also, oxide layers become more vulnerable to dielectric breakdown as their thickness decreases. In addition to technological advances in microelectronic fabrication, continued advances in the power output capabilities of microwave sources will also increase circuit vulnerability.

The study of circuit and device effects involves determining the port or input voltage transfer characteristics when these ports and pins are excited by HPM signals. On the system level, the objective is to establish how effects cascade throughout the large-scale systems and cause upset. In the literature electronic circuit and system upset levels are generally classified according to their severity. A commonly used and accepted classification is found in [17]:

- "*deny*"- Denial is upset caused by HPM signals that disrupt the function of a system for the duration of the event without causing any lasting damage to the system. The affected system will typically return to normal operation after the event. This type of disruption is also often referred to as *"jamming"*.
- *"degrade"*- Degrade is a very interesting classification. At this level of upset, the HPM signal still does little to no damage to the affected system's

components. However, the induced upset persists after the HPM event is over and the affected system must be reset to return to normal operation. An example would be an HPM event that causes a computer system to freeze, requiring that the system be rebooted. On occasion, this general condition is incorrectly referred to as *"latch-up"*, which is a very specific upset condition exclusive to CMOS devices.

- *"damage"*- Damage is one of two levels of upset that departs from the disruption of function from invading signals to the physical breakdown of materials that make up the system components. This level of upset will include device level oxide breakdown in MOS gates, bonding wire degradation due to thermal effects, etc. In terms of the total system, *"damage"* refers to a particular component of the affected system being damaged and needing to be replaced for the system to return to normal function. For example, if only an Ethernet card of a computer is damaged during and HPM event, the computer system itself will return to normal operation once the card has been removed or replaced.
- *"destroy"*- Destruction is the most severe upset HPM can cause to a microelectronic system. Destruction occurs when high levels of EM energy couple to a system and causes numerous components to suffer irreparable damage. The severity of the inflicted damage necessitates replacement of the entire system.

The upset classifications *"deny"* and *"degrade"* primarily deal with the circuit response to HPM signals. The study of these levels of upset will deal primarily with semiconductor device physics and circuit theory. In contrast, *"damage"* and *"destroy"* levels of upset involve the material properties of the system components such as the dielectric breakdown levels of oxide gates and thermal tolerances of bond wires.

1.3 Historical Overview

The work presented in this dissertation focuses on the study of the effects of HPM signals on the operation of CMOS circuits. This section contains a summary of the literature relevant to the study of electrometric interference effects in solid sate electronics.

1.3.1 Electromagnetic Interference Research

Some of the earliest work concerning electromagnetic interference effects in digital integrated circuits was conducted in the late 1970's. The prevailing device technology at the time was the bi-polar junction (BJT) transistor based TTL logic. Work conducted by Richardson [2, 21, 22] investigated the ability of microwave signals to shift the quiescent operation point of a bipolar junction transistor. Richardson demonstrated that low level RF signals are rectified by the nonlinear response of the emitter-base junction. An interesting result of this work was that, although the rectification response decreases with frequency, frequencies several orders of magnitude above the transition frequency of the device were also rectified. Larson and Roe [23] developed a modified Ebers-Moll transistor model capable of worst case scenario prediction of low level rectification effects in BJT's. Whalen *et al* used the modified Ebers-Moll model to perform susceptibility analysis on 7400 TTL

NAND gates using SPICE [24]. He demonstrated that RF injected at the input was capable of shifting the DC output level above or below the noise margins resulting invalid logic states.

In the 1980's the emphasis shifted to field effect transistors, as CMOS emerged as the preferred technology for digital integrated circuits. The first susceptibility analysis of a MOS device was published in 1981 by Roach [25]. In this study he characterized the susceptibility of NMOS memories. A very important work published by Kenneally [26] investigated the influence of electrostatic discharge (ESD) protection circuits on device susceptibility to EMI. Kenneally performed both experiments and computer simulation on a protected and unprotected D-type flip-flop and 8086 microprocessor. He demonstrated that EMI susceptibility decreases by approximately 40 dB as the RF frequency is increased from 5 MHz to 300 MHz. The maximum switching frequency of the device was approximately 5 MHz, which suggests that CMOS electronic devices are more susceptible to RF interference within their normal operating band. He also showed that ESD protection circuits can potentially increase device susceptibility, and that the more advanced 8086 processor was more susceptible at higher interference frequencies, which suggests susceptibility frequency ranges increases with more advanced process technologies. Another work by Kenneally *et al* [27] presented experimental results on CMOS D-type flip flops that demonstrated greater susceptibility of the clock terminal by as much as 20 dB higher than that of the V_{dd} power terminals.

Tront [28] performed a very interesting analysis on the typical input and output stages of CMOS digital IC's using SPICE2 simulations. The circuit

configuration for these experiments involved an output driver stage connected to an input buffer circuit, which would be typical of a data line between two independent IC's. RF signals of frequencies ranging from 80 MHz to 260 MHz were injected on the line between the output and input stages and the RF amplitude was varied from 0 to 26 V. Tront showed that 3 effects occurred based on the level of RF injection. High levels of injection produced a state latching effect, which prevented the circuit from changing state in the presence of a normal logic signal. For medium levels of injection, multiple state changes were observed during times when none were expected. Low levels of injection increased the delay time of the circuit.

Throughout 1990's a significant amount of work on EMI was conducted by a group at the University of Toronto. Laurin [29] conducted studies on EMI effects in clocked digital circuits. He termed effects as either static, which are EMI induced logic transitions, or dynamic, which involves changes in propagation delay. He showed that changes in propagation delay can lead to timing violations in clocked circuits, which can also lead to system failures. Laurin *et al* [30] also developed a method for the prediction of EMI induced delays using linear steady sate frequency domain analysis that could be applied to large systems without requiring extensive computer resources. Wallace [31] performed experiments on various CMOS and TTL D-type flip-flops using short transient impulses at the device input terminals. By synchronizing the impulse with clock signal, Wallace showed that devices are more susceptible when interference occurs near the clock transitions.

Macleod performed very interesting work in her PhD dissertation [32]. She designed an apparatus to conduct EMI susceptibility stress testing of electronic circuit

boards. The testing technique and theory developed in this work is capable of locating weak components that fail due to EMI stress. She also expanded the theory of EMI-induced delay to include high frequency and transmission line effects.

1.3.2 HPM Effects Research

The previous section presented a summary of work on the susceptibility of electronics to stray microwave energy produced by the environment. This section highlights work specifically focused on the intentional use of focused HPM to disrupt microelectronic systems. A great deal of work in this area is not available in the public domain due to the inherent defense applications of HPM technology [3]. The following overview presents HPM research centered on civilian applications and susceptibility of electronic systems vital to civil infrastructure.

The conventional method of assessing HPM susceptibility presenting in the following literature is the use of empirical testing. In the early 1990's, Pesta *et al* [33] proposed a standardized method for microelectronic system susceptibility assessment. He describes a methodology comprised of extensive low power microwave tests to measure EM coupling data to systems leads such as wires and board traces, and to assess the upset thresholds of individual system components. The collected data is used to create a database of susceptibility levels for the system under test. The second component of the method involves limited high power microwave testing to validate the database.

A group at the University of Hanover in Germany published several studies based on empirical testing of electronic equipment when exposed to ultra-wide band HPM pulses. In one study, Camp *et al* [9] performed susceptibility studies on

microcontroller circuits, where failure rates were measured as a function of the signal line length and HPM pulse rise time. They were able to demonstrate correlation between line length, HPM pulse rise time, and susceptibility, and presented a statistical failure distribution function for the prediction of susceptibility based on the external field strength. A similar study was conducted on personal computers with several generations of Intel processors ranging from the 8088 to the Pentium III [7]. The computers were subjected to UWB HPM pulses with rise times that ranged from 100 ps to 10 ns, pulse widths of 2.5 ns to 1.6 μs, and amplitudes that ranged from 25 kV to 1 MV. As reported by the authors, the major result of this study was that susceptibility increases substantially with newer computer generations.

Bäckström *et al* with the Swedish Defense Research Agency published a comprehensive work which presents a summary of a decade's worth of HPM testing conducted at the Swedish Microwave Test Facility [5]. HPM effects tests were conducted on various military and civilian systems such as tactical radios, automobiles, computers, etc. The journal article reports many useful general susceptibility trends including the following: Effects are more prominent in the L and S band range (1 GHz to 4 GHz), upset thresholds for systems usually occurs at few hundred volts per meter, and permanent damage begins to occur at field levels of 15 to 25 kV/m and that damage can occur when the system is turned off. Other tests were conducted to determine the effective upset range of different HPM sources.

An interesting study was performed by collaborative effort between Kim *et al* at the University of Maryland and Bayram *et al* at Ohio State University [6]. The work involved HPM testing of a digital timer circuit used for spark plug sequencing

in an automobile. The results of this study showed that even though automotive structures provide significant metal shielding, HPM induce upset can still be achieved using with reasonably achievable power levels. The study also successfully incorporated numerical EM analysis with conventional high frequency circuit simulation techniques to model and evaluate the system under test.

1.3.3 Focus of Recent Research Efforts

Recent efforts at the University of Maryland, as part of the Multidisciplinary University Research Initiative (MURI) from 2001 to 2006, began to investigate HPM effects with a new approach. The intention of the MURI project was to conduct research on a basic level in order to determine the physical mechanisms whereby HPM pulses can upset or damage modern integrated circuits, and to develop models and methodology to enable the design of HPM resistant microelectronic systems. Using innovative techniques, this research began the development of methods for evaluating HPM effects that are more effective and produce deeper insight then purely empirical methods.

One project during the MURI was focused on the difficult problem of evaluating induced voltages for objects inside complex enclosures such as computer cases and aircraft cockpits. As was noted previously, wavelengths at microwave frequencies tend to be very small compared to the dimensions of enclosures that contain microelectronic systems. Electronic enclosures also tend to have complex geometries where field distributions are highly sensitive to frequency and small perturbations. This makes deterministic evaluations of the field distributions with any degree of precision virtually impossible [34].

A statistical approach was developed to overcome the difficulties in describing fields in complex microelectronic enclosures. The result of this effort was computational model known as the Random Coupling Model (RCM) [34-37]. RCM is capable of predicting the probability density function (PDF) of voltages induced at a targeted electronic component within an enclosure. This calculation is possible with knowledge of the following basic parameters: the radiation impedance of the ports of the enclosure, the radiation impedance of the targeted electronic component, the volume and approximate loss characteristics of the enclosure, and the frequency of the incident waveform [34-37]. RCM has been extensively tested on both idealized enclosures and computer cases. Figures 1.2 and 1.3 show an example of the success of the RCM [34-37].

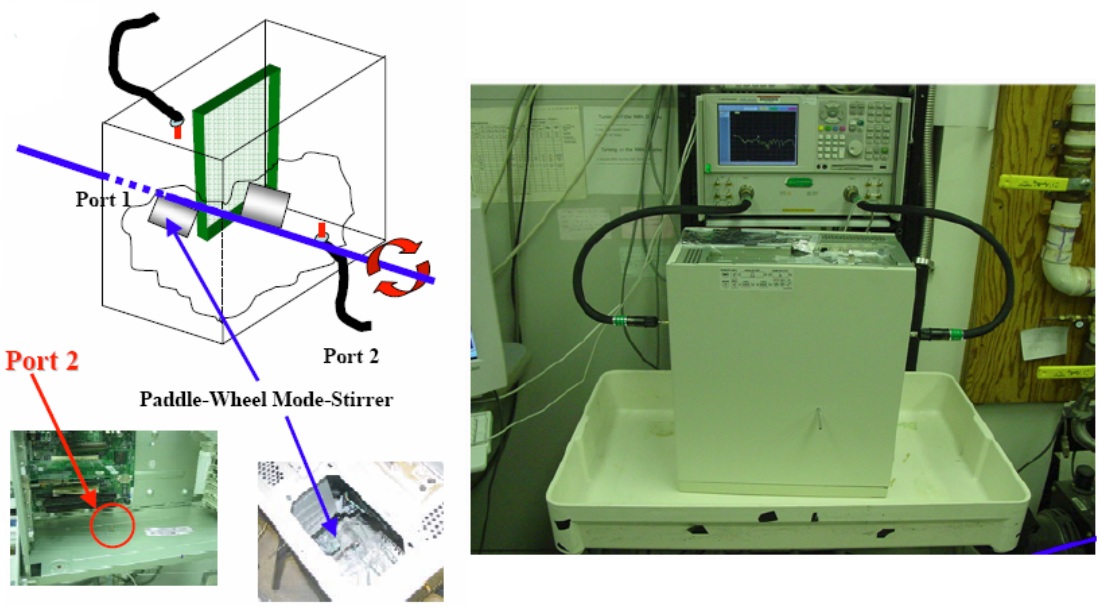

Figure 1.2: Example of experimental verification of the RCM on a computer case. Port 1 antenna broadcasts the attacking waveform while the statistics of the induced voltage were measured at Port 2[34].

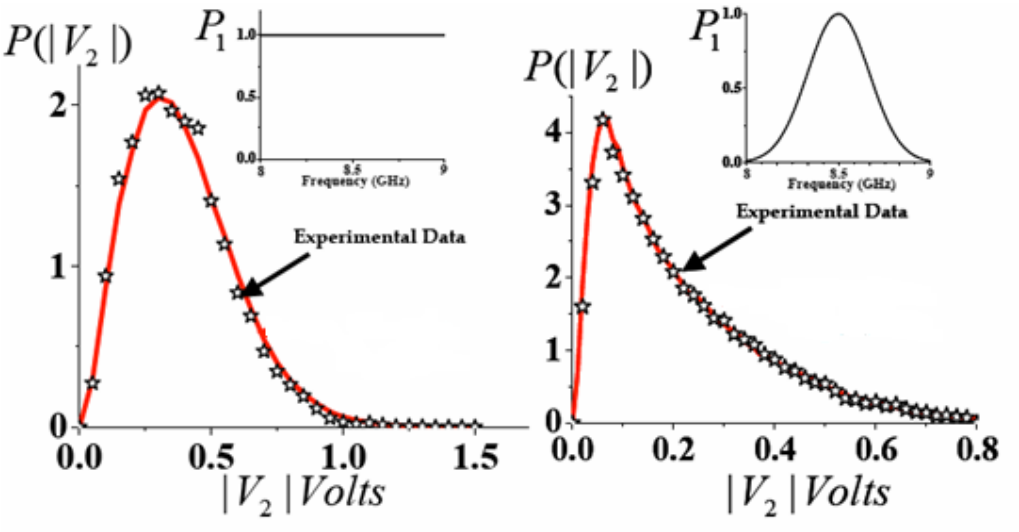

Figure 1.3: Measured PDF of induced voltages at PORT 2 versus the PDF predicted by the RCM for frequency range of 8 to 9 GHz. The plot on the left is for a flat power spectral density (PSD) and the figure on the right is for a Gaussian PSD[34].

In the experiment, the paddles created perturbations in the boundary conditions and mix the modes within the computer cases. The results in figure 1.3 and other experimental verifications show that the RCM accurately predicts the voltage PDF for a given port. Overall this research has produced very promising success and shown great potential for the statistical modeling of HPM fields inside complex enclosures.

Another part of the MURI program studied how HPM signals affected the operation of integrated circuits. Early studies performed on commercial IC's revealed that HPM can produce complex dynamics in circuits that result in bit errors, spurious oscillations, and undefined logic states. Figure 1.4 highlights two of the important overall results from measurements performed on a commercial CMOS inverter [38].

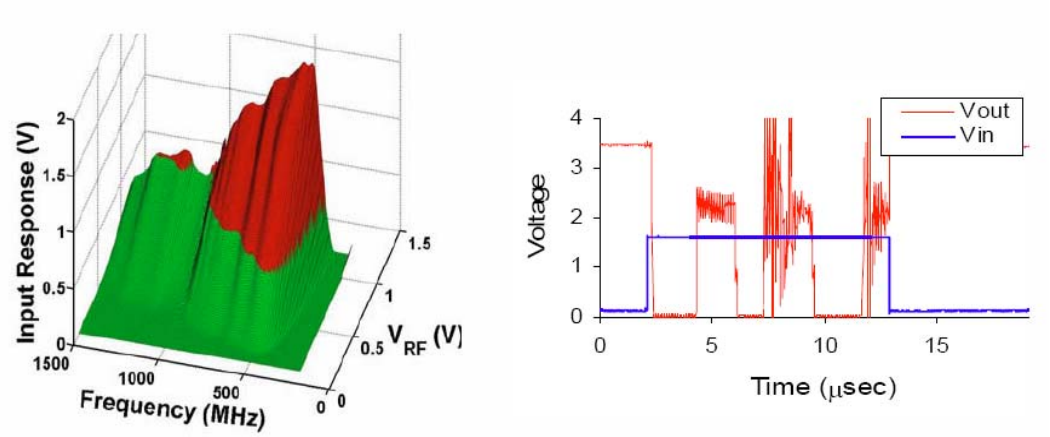

Figure 1.4: Input voltage response (left) and output waveform (right) for a commercial CMOS IC excited by HPM[38]

The figure on the left demonstrates that the input parasitic impedances greatly influence the actual voltage amplitude at the gate of the device. The red shaded region is where the input voltage levels are higher than the RF amplitude voltage due to resonant voltage gain. On the plot on the right, the blue trace represents the HPM pulse envelope as it corresponds to the output voltage, which is represented by the red trace[38]. The output voltage demonstrates the complex dynamics observed when HPM was injected into the commercial inverter. Results such as these were common with many different commercial ICs.

The observations from experiments on commercial devices prompted two parallel efforts to further study the complex circuits dynamics provoked by HPM interference on a more fundamental level. Both of these projects made use of custom fabricated devices designed specifically to measure the effects of HPM signals on normal device operation. One effort studied the influence of HPM on basic IC units such as individual MOSFETs and CMOS inverters. The key results of these experiments are the demonstration of HPM influence on device output current,

transistor transconductance, output conductance, and breakdown voltage. Another very important observation was that HPM effects diminished greatly at frequencies above 4 GHz [39-41].

The second research effort focused on the influence of electrostatic discharge (ESD) protection devices on circuit behavior when excited by HPM [42]. Previous studies have speculated that ESD protection devices play a central role in HPM effects. ESD devices typically take the form large PN junction diodes and are present in most commercial IC's. The devices are meant to prevent damage to the core circuit during incidents of electrostatic discharge. Aside from some passive loading, ESD devices are designed to have marginal influence to normal circuit operation. However, when excited by sufficiently large voltage amplitudes the devices can produce a significant DC component at the input of the core circuit thereby enhancing device susceptibility [42]. The experiments in this study were performed on specially designed structures that allow the ESD devices to be measured directly on the silicon chip using specialized precision RF probes. An example of one of these structures is shown in figure 1.5.

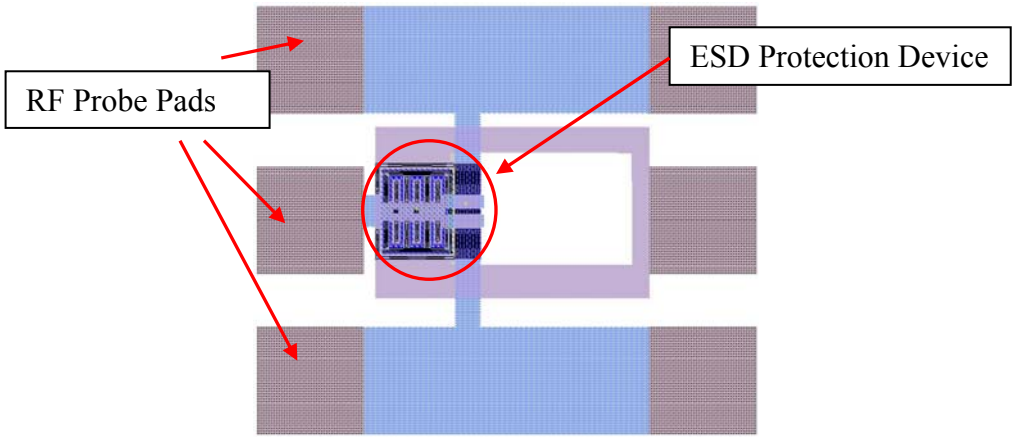

Figure 1.5: Example of a test structure used to measure the behavior of ESD devices when influenced by HPM signals[42]

Extensive measurements on ESD protection devices were performed and revealed that the nonlinear response of the drain to body PN junction greatly enhances HPM effects in simple CMOS inverters for frequencies from 100 MHz to 4 GHz. The characterization of these devices revealed that, at higher HPM frequencies, transient PN junction voltages are not accurately described by simple rectification based on quasi-static approximations [42]. This work also presented preliminary efforts to deterministically model HPM effects in basic devices using scalable physical parameters.

1.4 Project Overview

The research presented in this work is part of a larger effort to develop a foundational method for accurately predicting probability of effect in microelectronic systems when illuminated by HPM. The objective is build on the successes of the work presented in section 1.3.3 and contribute to the effort to combine statistical prediction of terminal voltages of devices in complex enclosures with deterministic circuit models that accurately predict HPM effects thresholds. This dissertation

details the results of experimental research performed to study the fundamental mechanisms responsible for HPM effects CMOS circuits, and the development of accurate deterministic modeling techniques to improve effects prediction capability.

Chapter 2 of the dissertation presents the design methodology and performance verification of the custom CMOS ICs created for this study. Chapter 3 details the experimental method for injecting HPM signal in to CMOS test circuits and the instrumentation arrangement used to accurately measure circuit response characteristics. Chapter 4 focuses on the input stage of the test circuits exploring in detail the response of the ESD protection devices and relating experimental observation to the relevant device physics. Chapter 5 contains the experimental measurements of the voltage and current characteristics for each of the test circuits, and the analysis of the experimental results used to determine the fundamental dynamics of the observed HPM effects. Chapter 6 presents the modeling techniques used to predict HPM effects thresholds and circuit behavior, and compares simulation results with the experimental measurements. Chapter 7 contains the summary discussion of the research effort and the near term future worked. Highlights of accomplishments in this work include:

1. Development of effective experimental methods for evaluating HPM effects in integrated circuits.
2. Evaluation of circuit input response characteristics based on semi-conductor device physics.
3. Identification of fundamental dynamics involved in observed HPM induced output voltage characteristic in digital CMOS circuits.

4. Identification and characterization of abnormal current behavior in CMOS circuits due to HPM effects.
5. Successful HPM effects prediction of CMOS test circuits using compact circuit models based on scalable physical parameters.
6. Demonstration of a technique for HPM effects prediction of non-quasi-static device behavior in ESD protection circuits that can be adapted to BSIM CMOS compact models.

Chapter 2 : Circuit Design

2.1 Test Circuit Overview

Previous efforts to characterize and model HPM effects in circuits and devices involved experimental evaluation of commercial devices and the use of either basic spice models or models provided by the manufacturer [28, 38]. These spice models are very simple, and in some cases are merely look up tables. Most of the compact model parameters and circuit topology is not made available due to proprietary restrictions. In order to avoid these restrictions, custom designed circuits were fabricated for this work. Custom circuits allow for exact knowledge of all significant parameters that are critical for accurate simulation efforts. All of the analytical model parameters extracted from the process test wafers are also available for each of the test circuits. The general philosophy for the test circuit design is to create basic CMOS circuits using established design principles, which are very similar in structure to their commercial counterpart. Fabricating custom test chips also facilitated measurement of the various stages of a circuit as isolated blocks and as an interconnected system. Thus susceptibility to HPM could be studied in terms of how effects cascade through circuits.

The following chapter details the design process for creating the test circuits used in this study. Test circuits were designed using Cadence Virtuoso layout tools and fabricated on the AMI (On Semiconductor) 0.6 μm process, available through the MOSIS service[43]. The test circuits are all comprised of four basic elements: ESD protection circuits, input buffer, core logic, and output buffer as depicted in figure 2.1.

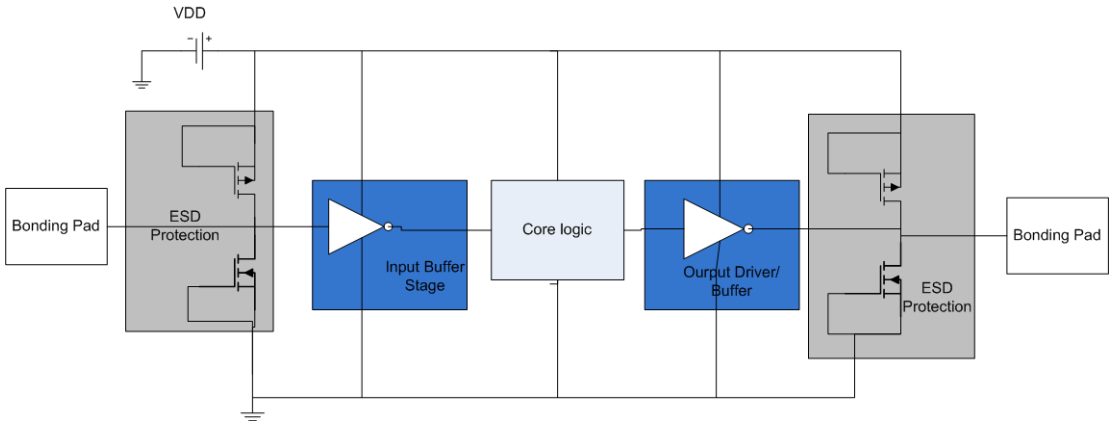

Figure 2.1: General test circuit topology

2.2 Basic Logic Gate Design

2.2.1 Design and Layout

This section covers the design of the core logic circuits. In order to create a series of digital test circuits, a basic digital standard cell library was designed consisting of the following logic gates:

- NOT (inverter)
- NAND two input – (AND two input)
- NAND three input – (AND three input)
- NOR two input – (OR two input)
- NOR four input – (OR four input)

The complement of the NAND and NOR gates are created by combining each with a NOT gate. Each cell is made with a standard spacing 13.95 µm between parallel ground lines and V_{dd} lines to make combining logic gates structurally simple and orderly. Each transistor is designed with the minimum gate width of 0.6 µm. The widths of each MOS device are kept as small as possible. The ideal switching point

for CMOS is $V_{dd}/2$, which balances the noise margins and ensures the best performance. To accomplish this, the switching characteristics and hence the current characteristic of the NMOS and PMOS should be balanced. The difference in NMOS and PMOS switching characteristics lies in the effective switching resistance defined by equation 2.1 [44].

$$R_{n,p} = \frac{2L \cdot V_{dd}}{k_{n,p} W \cdot (V_{dd} - V_{th})^2} \tag{2.1}$$

V_{th} is the threshold voltage, and W and L are the gate width and length respectively, and the term k is defined by equation 2.2.

$$k = \mu_{n,p} C_{ox} \tag{2.2}$$

$\mu_{n,p}$ is the surface mobility of electrons and holes respectively. C_{ox} is the gate capacitance per unit area. The effective switching resistance of the NMOS and PMOS differs due to the term k and its dependence on mobility. In silicon, the mobility of electrons is approximately two to three times larger than the mobility holes. For this reason, the width of the PMOS is typically three times larger than the NMOS width in the initial design. However, this is based on approximation, and ignores most short channel effects. Thus, the width ratio should be adjusted to ensure the switching point occurs at $V_{dd}/2$.

During the design process, it was determined that a width ratio of 2:1 provided the optimal balance between NMOS and PMOS for the basic inverter. The widths of the other standard cells are also influenced by the number of MOSFETs in parallel or series compared to each transistors compliment. Transistors in parallel reduce the overall effective resistance while parallel connections increases it, and thus widths are

adjusted to compensate. The following figures are the schematics and layouts of each cell followed by Table 2.1, which summarizes the important physical parameters.

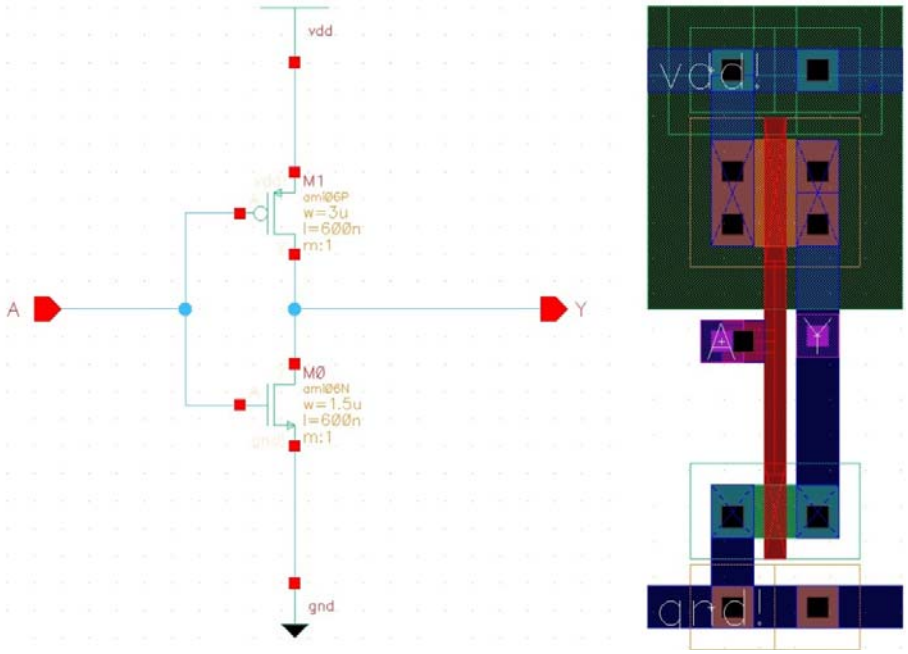

Figure 2.2: NOT gate schematic (left) and layout (right)

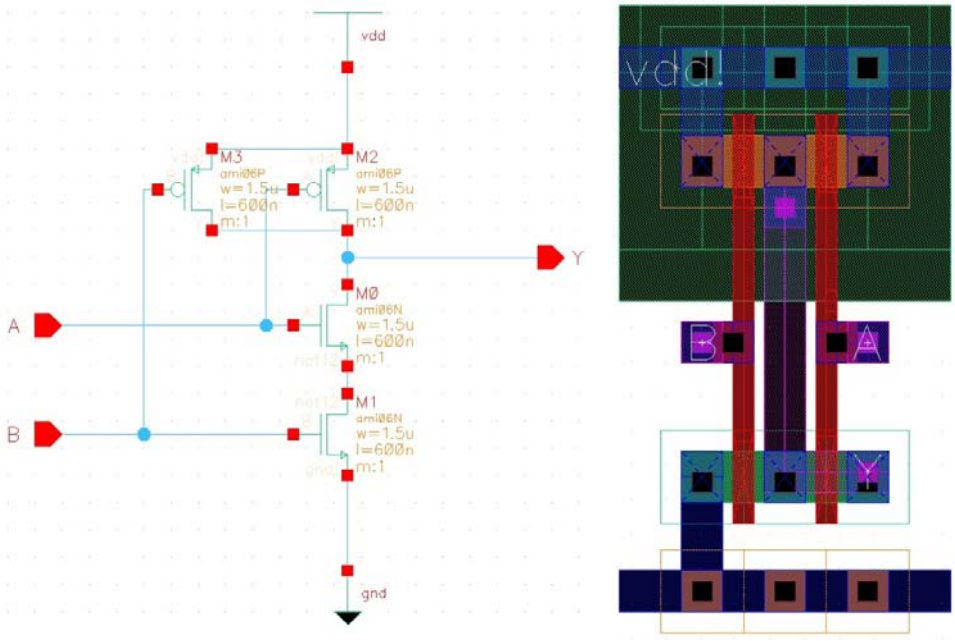

Figure 2.3: Two input NAND gate schematic (left) and layout (right)

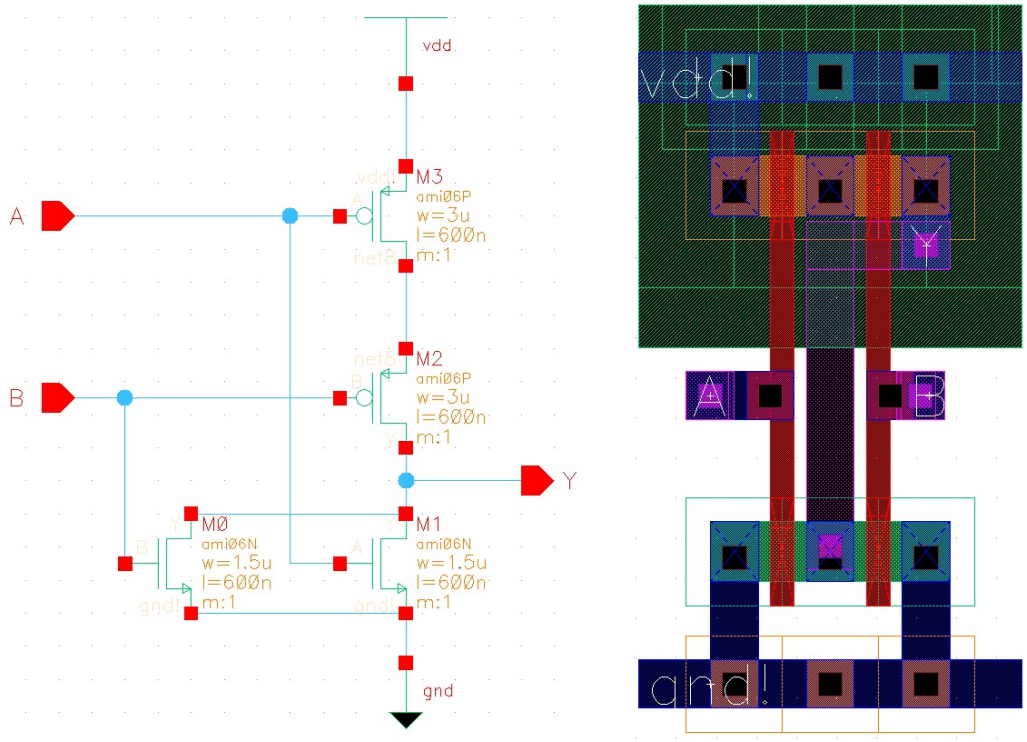

Figure 2.4: Two input NOR gate schematic (left) and layout (right)

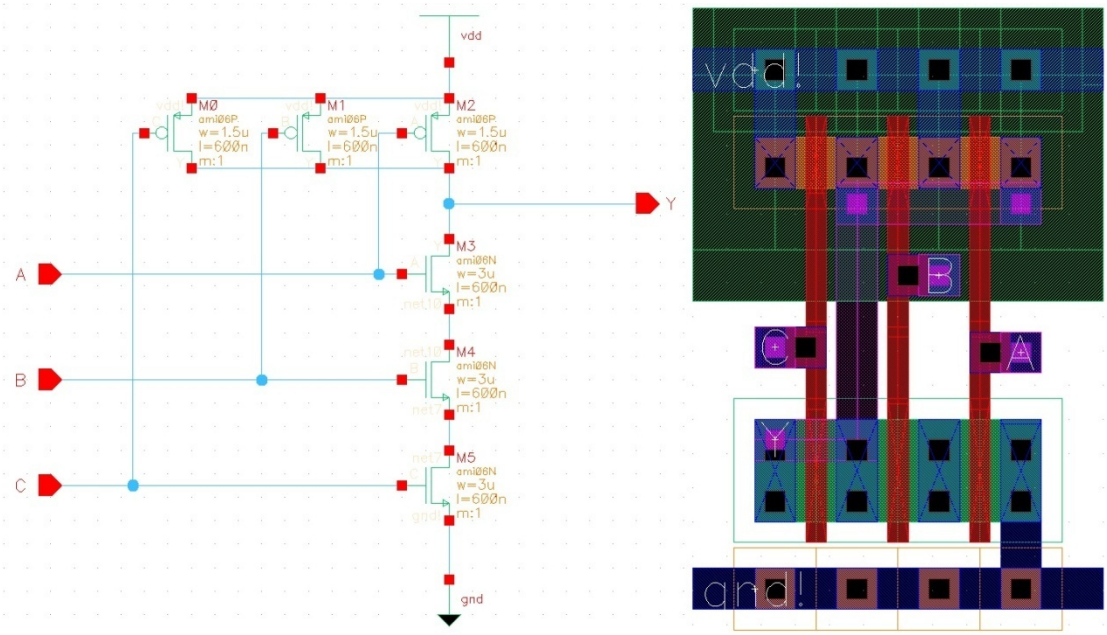

Figure 2.5: Three input NAND gate schematic (left) and layout (right)

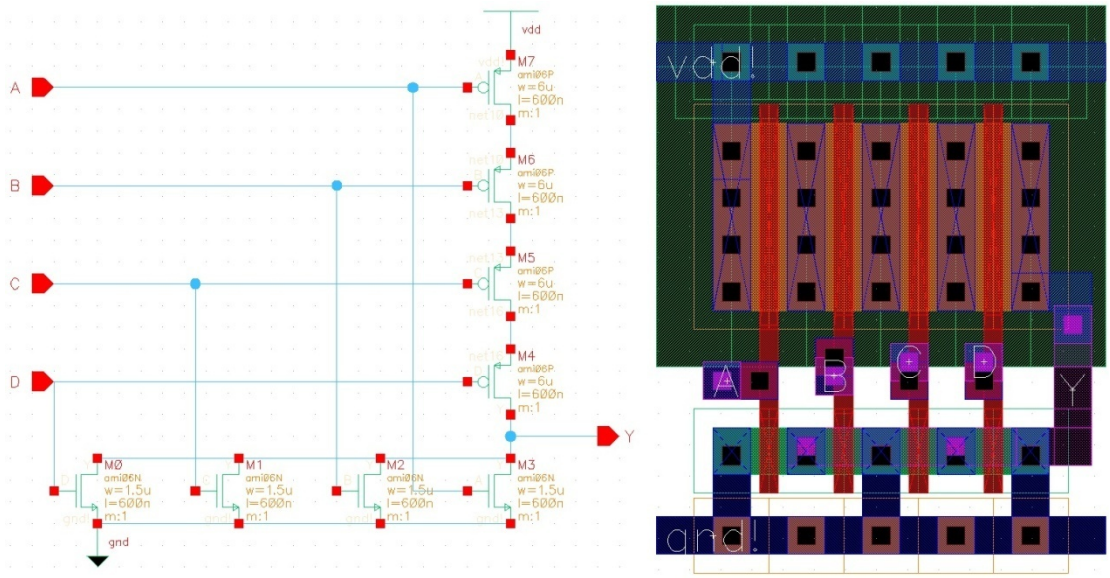

Figure 2.6: Four input NOR gate schematic (left) and layout (right)

Table 2.1: Physical parameters of basic logic cells extracted from the layout

	Gate Width (μm)	*Drain/Source Diffusion area (m^2)*	*Drain/Source Diffusion Perimeter (μm)*
NOT NMOS	1.5	2.25E-12	6
NOT PMOS	3	4.5E-12	9
NAND 2 NMOS	1.5	2.25E-12	6
NAND 2 PMOS	1.5	2.25E-12	6
NOR 2 NMOS	1.5	2.25E-12	6
NOR 2 PMOS	3	4.50E-12	9
NAND 3 NMOS	3	4.50E-12	9
NAND 3 PMOS	1.5	2.25E-12	6
NOR 4 NMOS	1.5	2.25E-12	6
NOR 4 PMOS	6	9.00E-12	15

2.1.2 Performance Evaluation

The following basic performance evaluation was conducted using Cadence Spectre circuit simulator. The purpose of the evaluations is to verify the basic design functionality and to assure the device operations conform to established circuit design standards [44, 45]. Extraction was performed on the layout of each circuit in order to include the parasitic capacitances in the simulations. An important performance measure for CMOS electronics in general are the noise margins [44, 45]. One of the greatest advantages to CMOS digital circuits over its junction transistor counterpart is its large noise margins. Consider the voltage transfer curve for the NOT gate in figure 2.6. Any voltage below red line marked V_{IL} is considered a valid logic low on the input of the inverter.

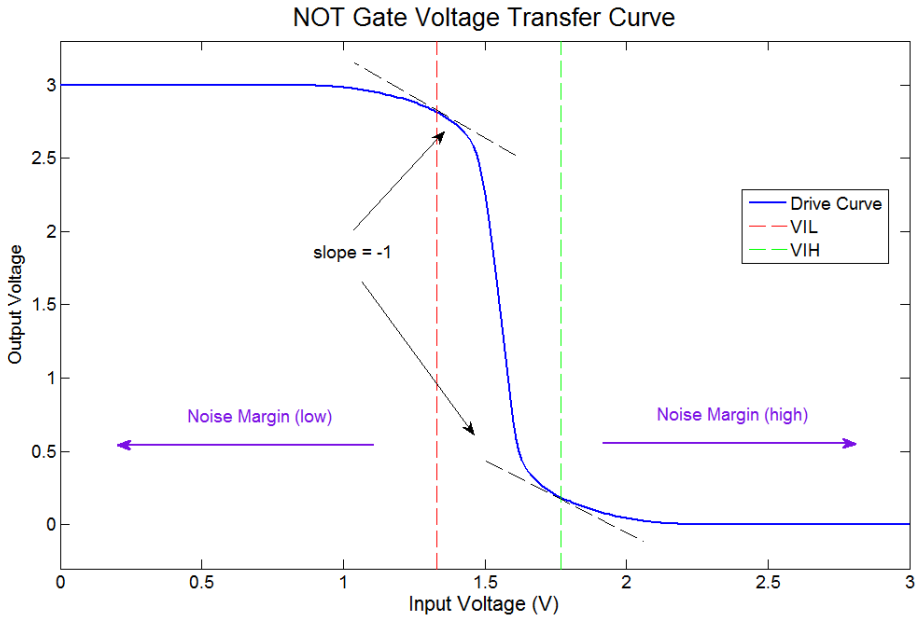

Figure 2.7: Plot of the voltage transfer characteristics of the NOT; Illustration of noise margin measurement

Any voltage above the line marked V_{IH} is considered a valid logic high on the input of the gate. V_{IH} and V_{IL} are defined by the point where the slope of voltage transfer curve is equal to -1[44]. In other terms, when the input of the circuit is logic low, the circuit can handle any voltage noise level at the input up to V_{IL} without changing state. The region in between V_{IL} and V_{IH} is considered an invalid logic state.

In addition to the noise margins, the peak transition current was evaluated for each gate. This is the current drawn by the CMOS circuit as it transitions from one state to another. The plot in figure 2.7 shows the drive curve for the NOT gate.

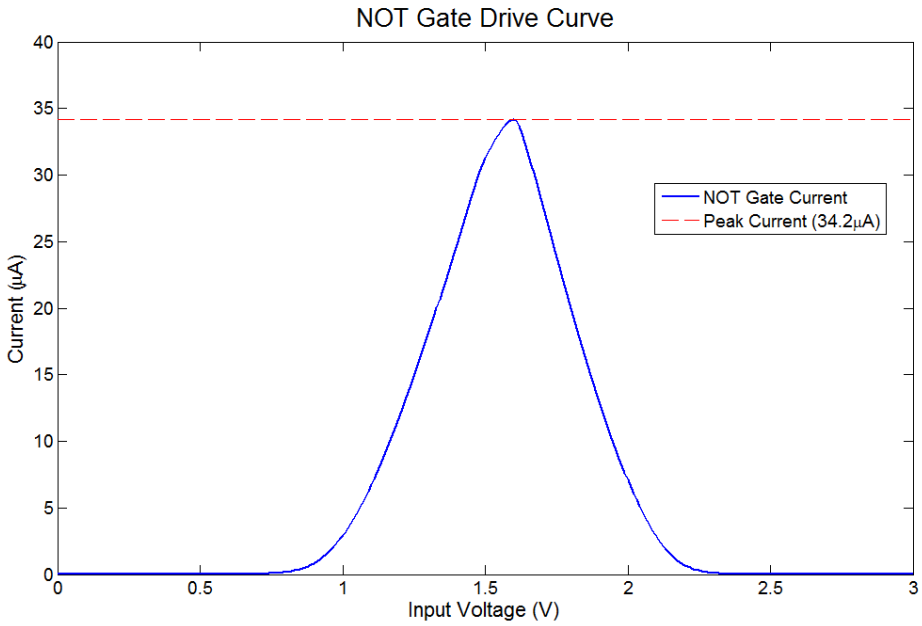

Figure 2.8: Current drive curve for the NOT gate

Table 2.2 contains the noise margin and peak current data for each of the gates in the standard cell library for Vdd equal to 3 V.

Table 2.2: Intrinsic device characteristics derived from SPETCRE simulations

	VIH (V)	*VIL (V)*	*High Noise Margin (V)*	*Low Noise Margin (V)*	*Peak Current (μA)*
NOT	1.77	1.33	1.23	1.33	34.2
NAND 2	1.65	1.25	1.35	1.25	20.4
NOR 2	1.66	1.23	1.34	1.23	28.2
NAND 3	1.59	1.25	1.41	1.25	33.6
NOR 4	1.78	1.31	1.22	1.31	44.2

2.3 JK Flip Flop and 4 Bit Counter Design

A JK flip-flop and 4 bit synchronous counter were designed as a representative digital test circuit in this study. The flip-flop was chosen because they are ubiquitous devices found in many computational and storage circuits such as synchronizers, registers, and counters [46]. The flip flop also provided the basic building block for the 4 bit counter and can be used as a building block for other computational test circuits in the future. The flip flop design utilizes 2 three input NAND gates, 6 two input NAND gates, and one NOT gate with total transistor count of 48 [46]. The device switches state on the negative transition edge of the input clock signal only when logic 1 is present at the *J* and *K* terminals. For the JK flip flop test circuits used in this study, the J and K terminal are permanently tied to the V_{dd}. This creates a T flip flop configuration where the state of the device is only controlled though the input clock signal.

One important question to answer in regards to HPM effects is how effects observed on simple CMOS circuits cascade through more complex circuits. A 4 bit synchronous counter was designed for this purpose. The counter represents a very common and basic computational digital logic component. The design consists of 4

JK flip flops, 1 two input AND gate, and 1 three input AND gate for a total of 202 transistors. The counter is controlled by an input clock signal and all four bits are available to output pins through the output buffer circuit to allow for independent probing. Figure 2.9 and 2.10 are the schematics and layouts of flip flop and counter circuits.

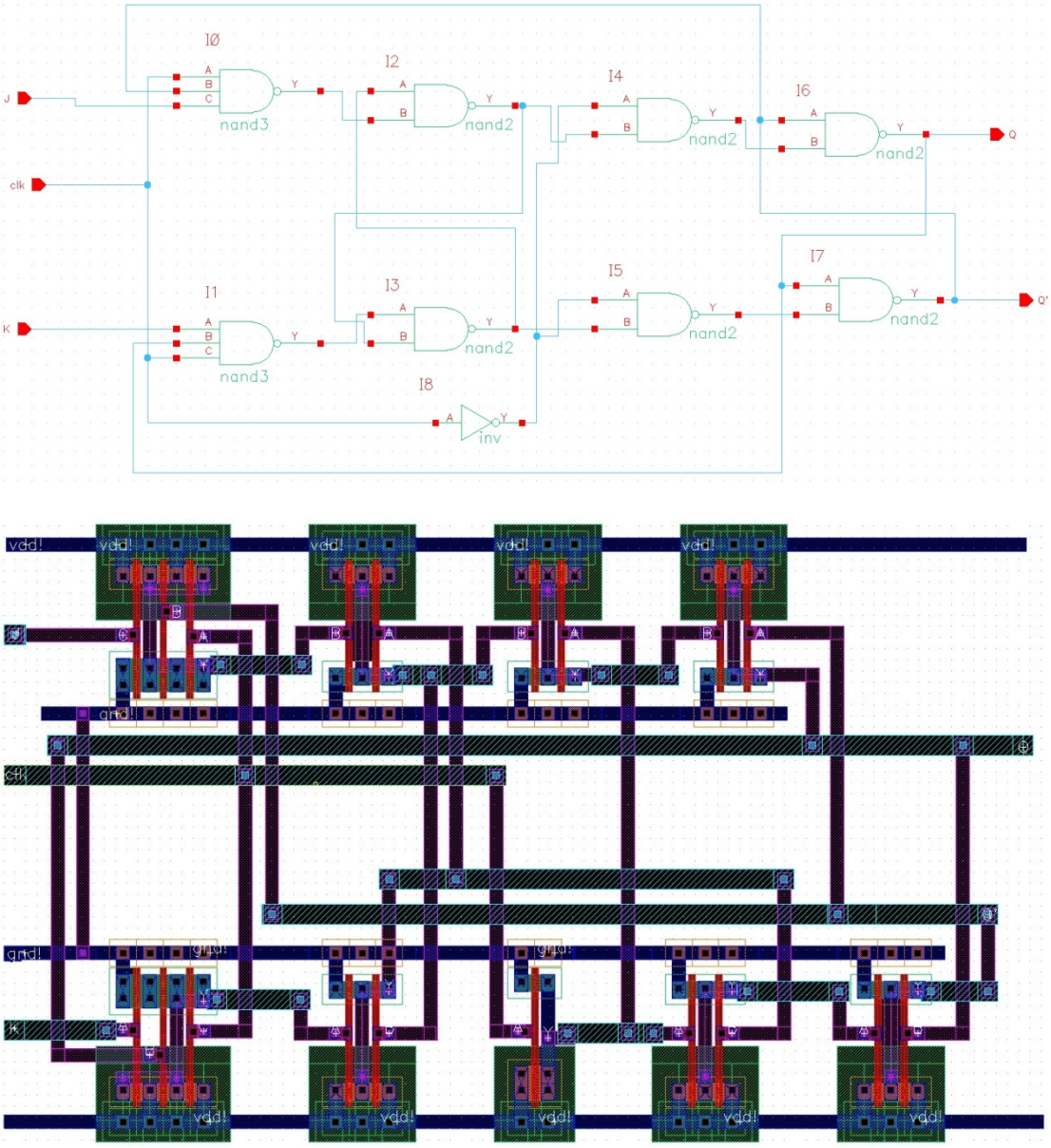

Figure 2.9: Schematic (top) and layout (bottom) of the JK flip flop test circuit

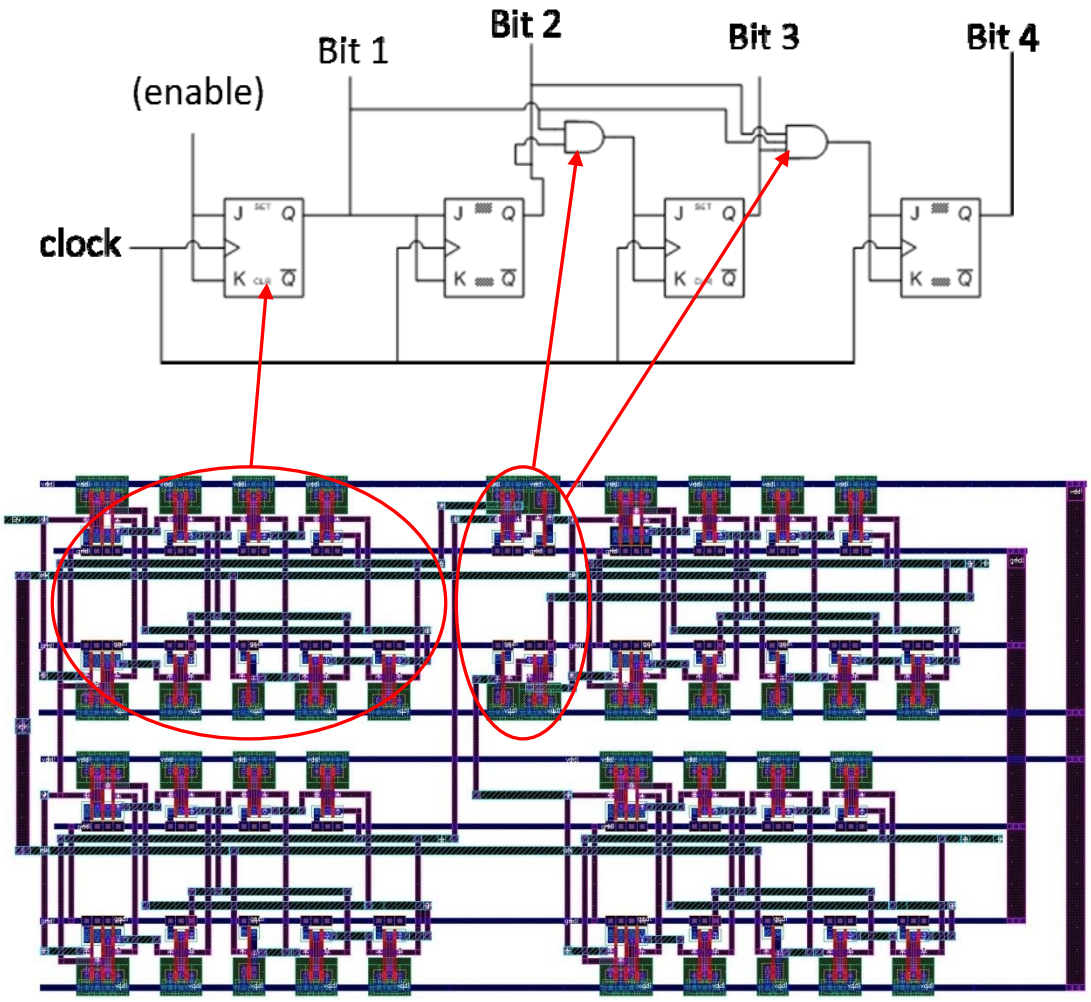

Figure 2.10: Schematic (top) and layout of the 4 bit counter test circuit

2.3 ESD Protection Circuit

ESD protection devices are essential elements in commercial IC's. One of the greatest reliability problems that face the IC industry is the loss of product yield due to ESD generated failure [47, 48]. ESD events occur when two oppositely charged objects are brought into close proximity of one another and charges transfer from object to the other very rapidly. Electrostatic discharges are an extremely fast phenomenon with durations of approximately 100 ns [47]. The resulting current can be as high as tens of Amps and the voltage on the order of kilovolts. When this transient event occurs on I/O pins of IC's, the result is often degradation or destruction of the device.

ESD protection devices are large dimension devices whose purpose is to provide a low impedance path in order to shunt high peak ESD currents to ground or through the supply rail, and to clamp the input voltage to a safe level to avoid input gate damage due to dielectric breakdown. The devices are fabricated directly onto the silicon chip just after the bonding pads to the I/O port of the IC [48]. ESD devices can present input and output loading problems to ICs, especially for more advanced very deep sub-micron process technologies. For this reason, many advanced ESD topologies inaccessible due to proprietary restrictions.

The ESD protection devices used in the test circuits designed for this study are the gate grounded NMOS (ggNMOS) and gate grounded PMOS (ggPMOS). These ESD devices are well known and commonly used in many commercial IC's [49]. The ggNMOS consists of a large dimension NMOS where the drain is connected to the

I/O pin and the gate is connected to ground along with the source. The ggPMOS is configured in the same manner with the exception that the gate is connected to V_{dd}.

The ggNMOS and ggPMOS take advantage of a parasitic bipolar junction transistor that is formed between the drain, source and body of the device as shown in figure 2.11[49].

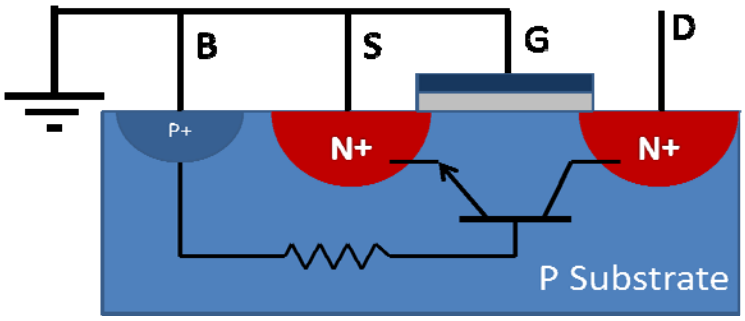

Figure 2.11: Cross section of ggNMOS ESD protection device showing the parasitic BJT

When a positive ESD pulse appears at the drain of the ggNMOS, the drain body junction is reversed bias until the avalanche breakdown voltage is reached. A hole current to ground through the body of the device is generated due to the impact ionization created by the breakdown phenomenon. This current creates a voltage drop across the body resistance. As the voltage increases, the source body junction will eventually forward bias. At this point the parasitic NPN BJT turns on, creating a low impedance path to ground away from the input gate of the protected circuit [49]. This process of triggering the parasitic BJT is referred to as *snap-back*.

The ggNMOS and ggPMOS used in the test circuits consist of a 12 finger MOSFET. The dimensions for the ggNMOS and ggPMOS are typically the same since the two transistors do not form a CMOS pair and hence there is no need to

balance switching characteristics. Figure 2.12 shows the layout of the ESD protection devices followed by table 2.3, which lists the dimensional parameters.

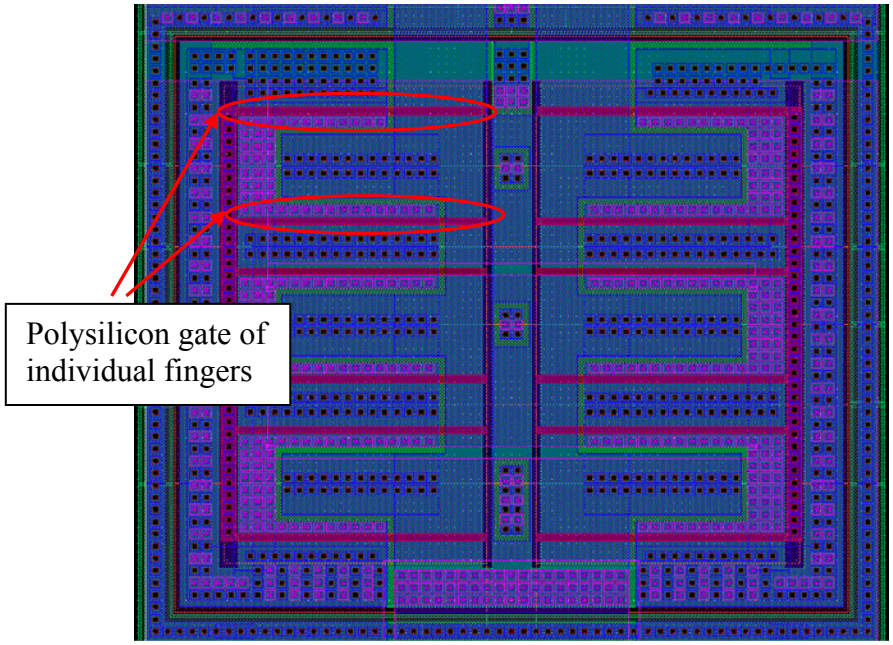

Figure 2.12: Individual gate grounded NMOS layout

Table 2.3: Dimensional parameters for the ggNMOS and ggPMOS per finger

Gate Width (µm)	Gate Length (µm)	Drain Diffusion area (m^2)	Drain Diffusion Perimeter (µm)	Source Diffusion area (m^2)	Source Diffusion Perimeter (µm)
30	0.9	1.845E-10	72.6	8.1e-10	65.4

The ESD protection devices are placed together with a metal bonding pad, and each individual ESD and bonding pad section fits together to form a pad ring as shown in figure 2.13.

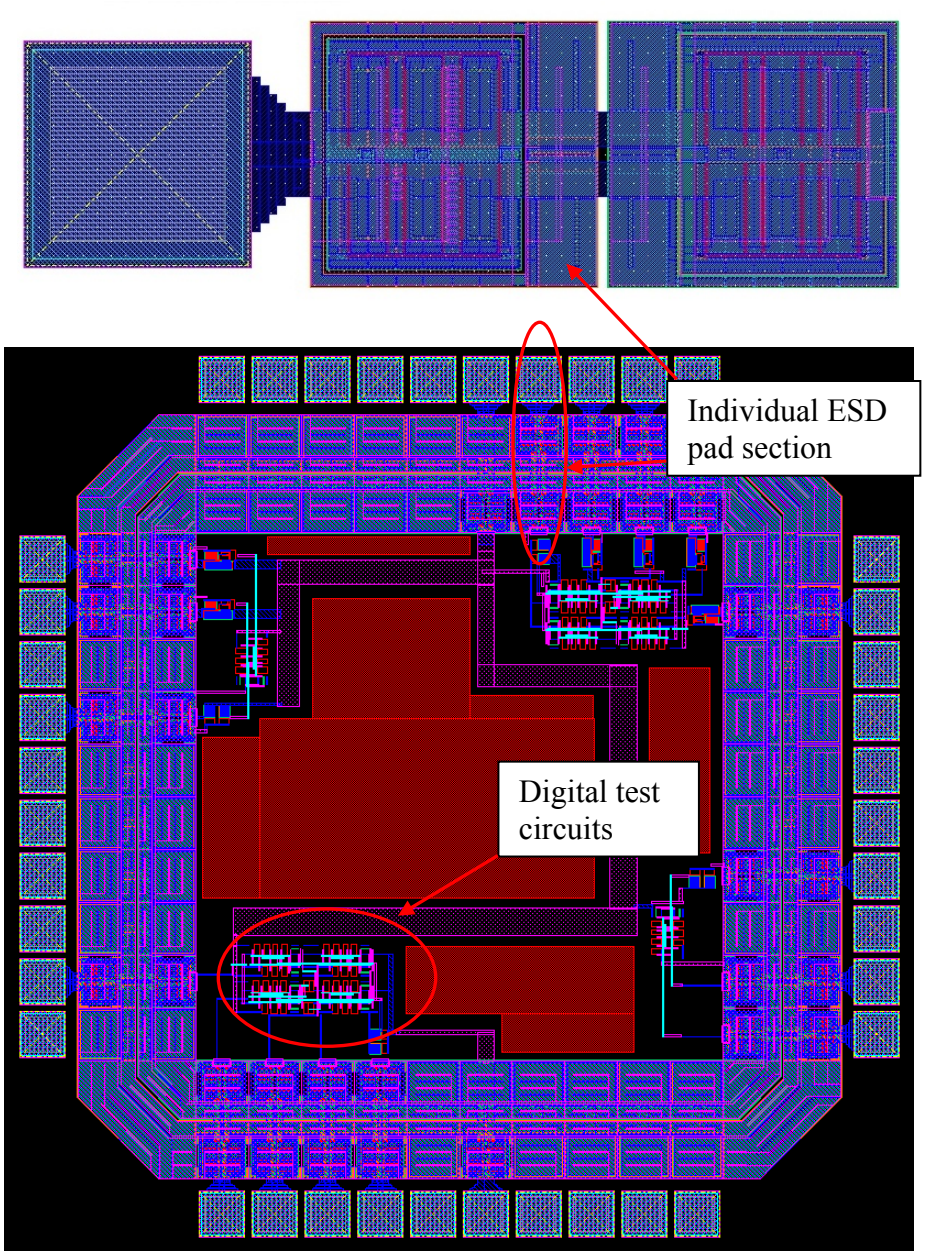

Figure 2.13: ESD protection ring and bonding pad arrangement for the digital test circuits.

2.4 Input and Output Buffer Circuits

2.4.1 Input Buffer

Input buffer circuits serve the purpose of accepting input signal to the chip and creating a clean signal to the logic circuits. Typically an input buffer will have very sharp voltage transfer characteristics (high dynamic gain) in order to sharpen any imperfections that may be on the input signal. The input buffer design chosen for this work is a simple two inverter stage buffer with each inverter having equal dimensions. The schematic and layout of the inverter used in the buffer circuit is shown in figure 2.14, followed by dimensional parameters in table 2.4.

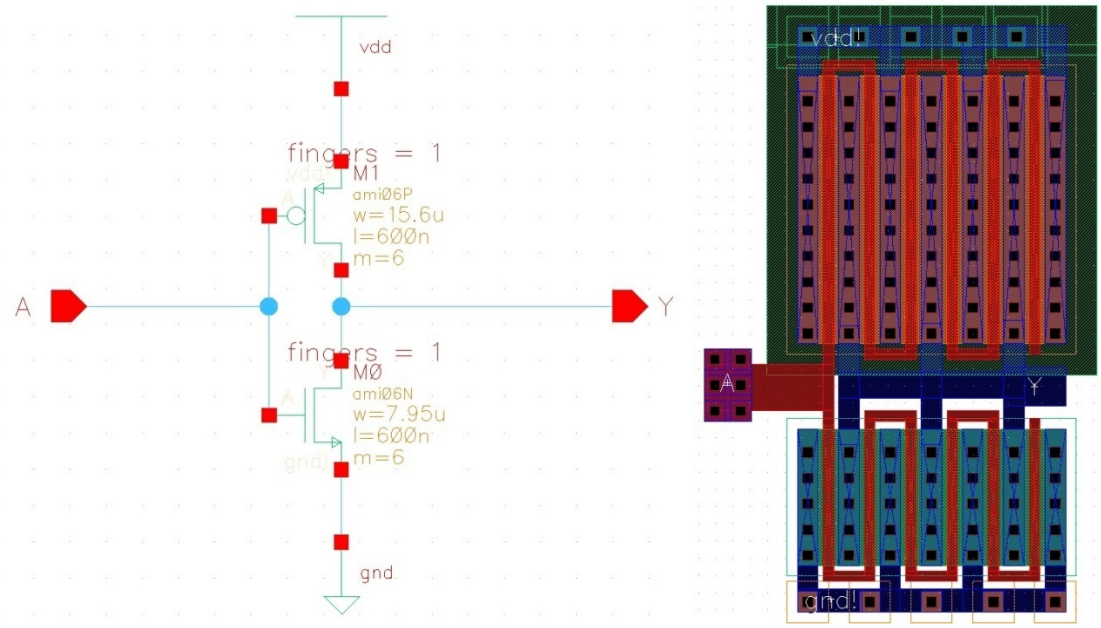

Figure 2.14: Schematic and layout of the inverter used in the input buffer circuit.

Table 2.4: Dimensional parameters for a single finger of the 6 finger inverter of the input buffer circuit.

	Gate Width (µm)	Gate Length (µm)	Drain/Source Diffusion area (m^2)	Drain/Source Diffusion Perimeter (µm)
NMOS	**7.95**	0.6	7.16E-10	113.4
PMOS	15.6	0.6	1.40E-10	205.2

The dimensions of the inverter circuit were optimized to create a sharp transfer characteristic centered at approximately 1.5 V. Figure 2.15 shows the voltage transfer curve of the buffer circuit obtained through Sprectre simulation. The blue trace is the voltage transfer curve of the first inverter stage and the red trace is the voltage transfer curve for the full circuit. As can be seen from the plot, the input buffer has very large noise margins with V_{IL} equal to 1.44 V and V_{IH} equal to 1.56 V.

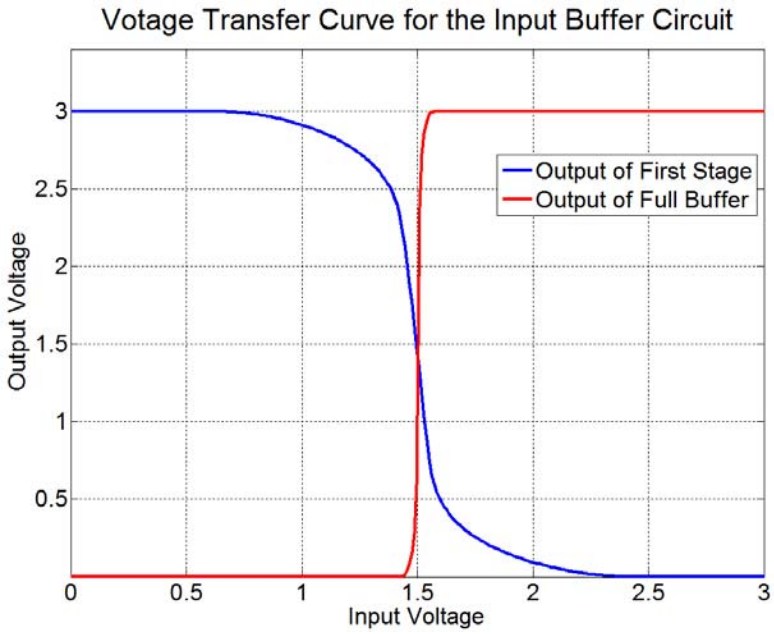

Figure 2.15: Voltage transfer curve for the input buffer circuit.

The typical load for the input buffer will be at the most on the order of 150 fF, which is the approximate maximum input capacitance of the digital test circuits. Figure 2.16 shows the results of the simulation of the input buffer with a 150 fF load. The input signal was given a slow rise time of 10 ns to demonstrate how the buffer circuit sharpens the rising and falling edges of the signal. The basic inverter based buffer is a common input circuit technique for simple systems. More complex input circuits are often employed in many larger systems to assure timing errors don't result from the input signal rise and fall times being sharpened [44]. However, for this study, the simpler buffer is adequate.

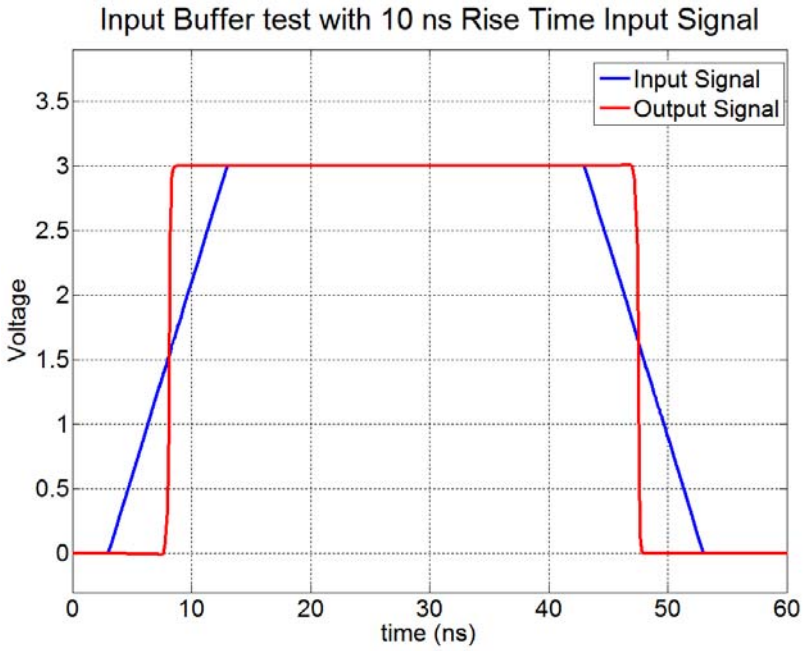

Figure 2.16: Transient simulation of the input buffer circuit.

2.4.2 Output Buffer

The output of the digital IC must be able to drive the total output load capacitance of the circuit. This capacitance includes the parastic capacitance from the ESD, the board trace, and the input capacitance of the circuits recieving data. For the

test setup used in this work the load capacitance will be as a high as a few picofarads. The digital elements described in section 2.2 are not capable of driving such high capacitances. This is typical of any circuit and the difficulty is overcome by proper design output buffer stage. The design goal of an output buffer is to be able to drive a large capacitive load while not substaintially contributing to the propagation delay [44].

The ouput driver used in the test circuit was design using a very common technique. The method involves designing an inverter string with each inverter's width larger than the previous inverter's by a factor "A", which is defined by equation (2.3).

$$A = \left(\frac{C_{load}}{C_{in1}} \right)^{\frac{1}{N}} \tag{2.3}$$

C_{load} is the load capacitance of the final stage and C_{in1} is the input capacitance of the first stage. The factor N is the total number of stages defined by equations (2.4).

$$N = \ln \frac{C_{load}}{C_{in}} \tag{2.4}$$

The concept is that the effective switching resistance of each stage is reduced by the factor A. The total switching resistance is therefor reduced by a factor of A^N [44]. As a result, each stage is capable of driving a larger capacitance and no one stage is driving a capacitance that causes a dramatic increase in the total propagation delay. The width and number of stages can be further optimized from the calculated values to minimize the delay. The output driver consists of 3 stages and the schematic and layout are shown in figure 2.17 and figure 2.18, followed by the dimensional parameters in table 2.5.

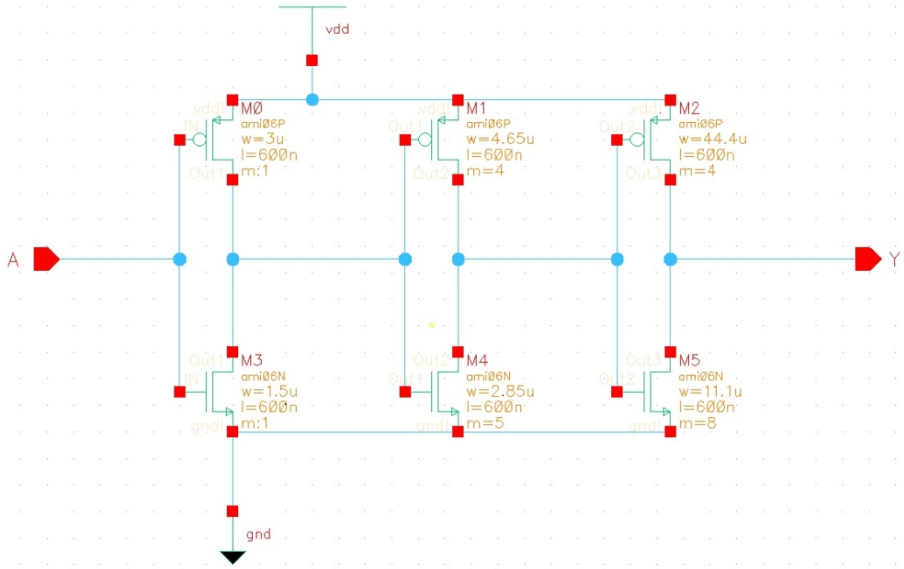

Figure 2.17: Output buffer schematic

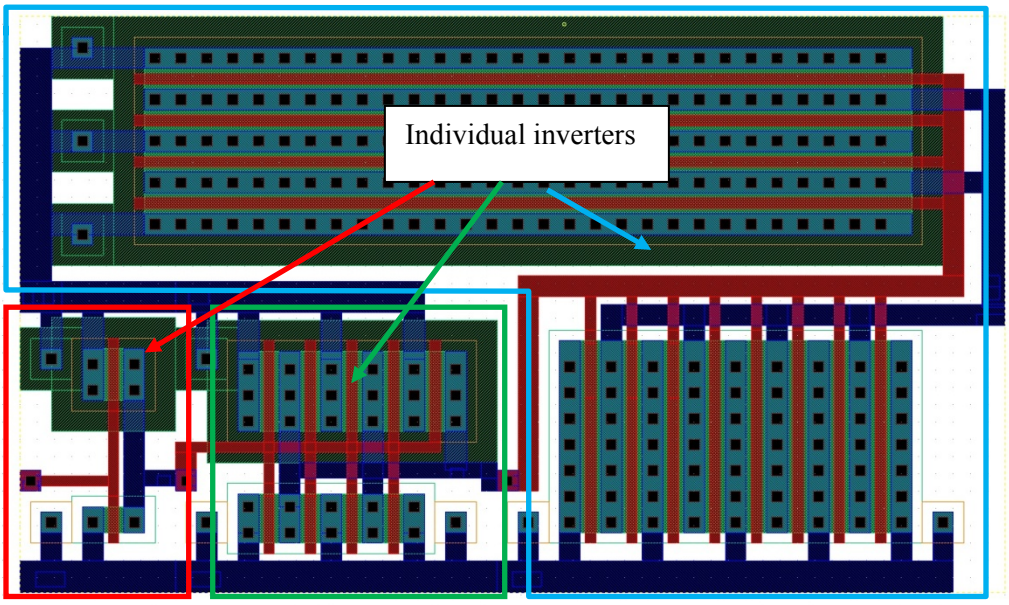

Figure 2.18: Output buffer layout

Table 2.5: Dimensional parameters for the output buffer circuit

	Gate Width (μm)	*Drain/Source Diffusion area (m^2)*	*Drain/Source Diffusion Perimeter (μm)*	*Number of fingers*
Inverter 1 NMOS	1.5	2.25E-12	6.0	1
Inverter 1 PMOS	3	4.50E-12	9.0	1
Inverter 2 NMOS	2.85	4.28E-12	8.7	5
Inverter 2 PMOS	4.65	6.98E-12	12.3	4
Inverter 3 NMOS	11.1	1.67E-11	25.3	8
Inverter 3 PMOS	44.4	6.67E-11	91.8	4

The dimensions of each inverter stage was optimized to be able to drive a 5 pF load, which is larger than the typical circuit load used in the experiments. Figure 2.19 shows the drive curve of the buffer circuit at each of its stages acquired from Spectre simulation.

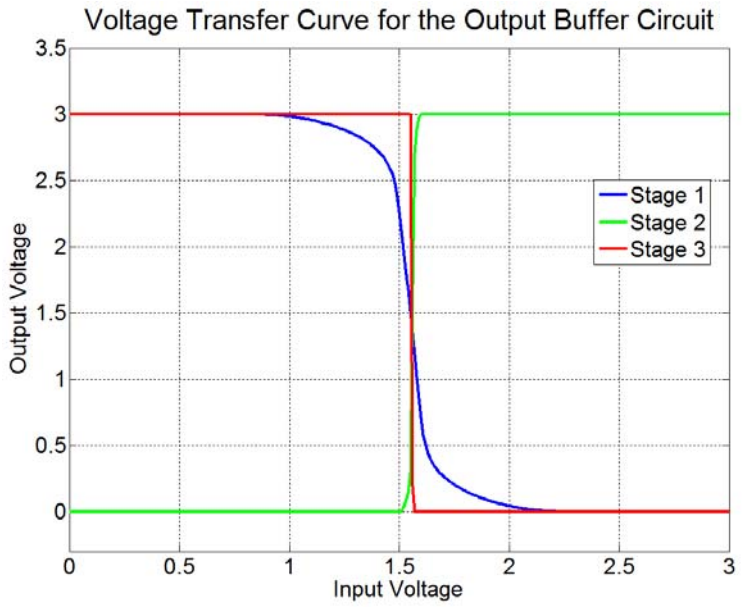

Figure 2.19: Voltage transfer curve for the output buffer circuit

Figure 2.20 shows the result of transient simulation of the output buffer with an input pulse signal with a 1 ns rise time and a load capacitance of 5 pF. The results predict a propagation delay of 1.6 ns, which is acceptable for the test circuits used in this study.

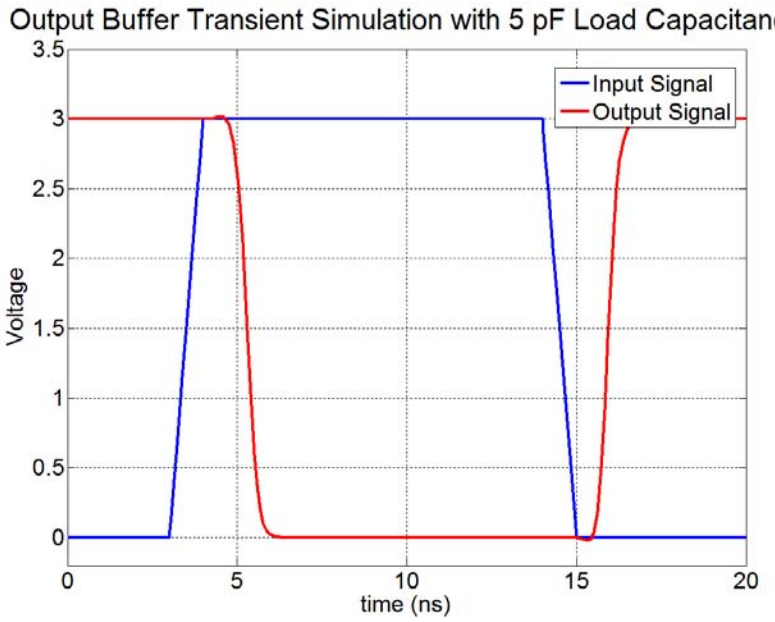

Figure 2.20: Input and output voltage waveform from transient simulation of the output buffer circuit.

The rise time of the output is approximately 1 ns, which demonstrates that the circuit will perform very well under the experimental load requirements.

2.5 Full Test Circuit Evaluation

This section presents the evaluation of the test circuits used in this study under normal operating conditions. The purpose of this evaluation is determine the maximum digital operating frequency of each circuit and the average current drawn within the normal operating band of each circuit. This distinction is important because HPM signals may be inside the normal operating range or far beyond it. As

will be shown in later chapters, circuit effects can be better understood when the operating limits of the circuit are known. .

The following test circuits are assembled as shown in the general circuit in figure 2.1:

- single NOT gate (inverter)
- JK flip flop
- 4 bit counter

In addition to these circuits, an individual inverter circuit without any buffer stages was independently fabricated. This single inverter test circuit is the same inverter used to construct input buffer shown in figure 2.14. The single NOT gate circuit will be referred to as the "inverter chain circuit" since it consists of 6 total inverters including the buffer stages. This is to avoid confusion with the single inverter test circuit. Each chip is packaged in a LCC 44 surface mount carrier and the chips were mounted to a test printed circuit board. A digital input signal was generated by a Tektronix AWG5014 arbitrary waveform generator. The signal generator is capable of producing a digital waveform with frequencies up to 100 MHz. Probe points were soldered as close as possible to the input and output pins, and Tektronix TAP1500 oscilloscope probes were connected in order to measure the input and output signals. The input and output probes were fed to a Tektronix MSO 4104 mixed signal oscilloscope. The power supply voltage was set 3 V to provide the rail voltage. A Keithley model 6487 picoammeter was connected to the current return path to measure the average current. The complete experimental setup is show in figure 2.21

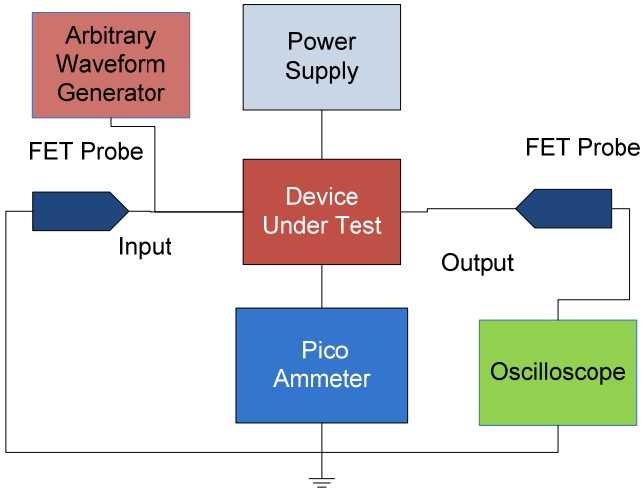

Figure 2.21: Measurement setup for test circuit performance evaluation

The first measurement performed was to verify the basic functionality of each of the test circuits. The propagation delay was measured and used to determine the upper operational frequency limit of each test circuit. The frequency limit is assumed to have a period equal to the delay. The delay measurements were performed by measuring the time difference of the input rise and the output rise at the point where they are both at 50% of V_{dd} [44]. The same measurement is performed for the input and output fall times and the two delay times are averaged to obtain the propagation delay.

For current measurements, the input frequency was swept from 1 MHz to 100MHz and the pulse width was maintained at one half the periods for each frequency to ensure maximum switching and congruence between each frequency. The results of the current measurements are presented in the plot in figure 2.22.

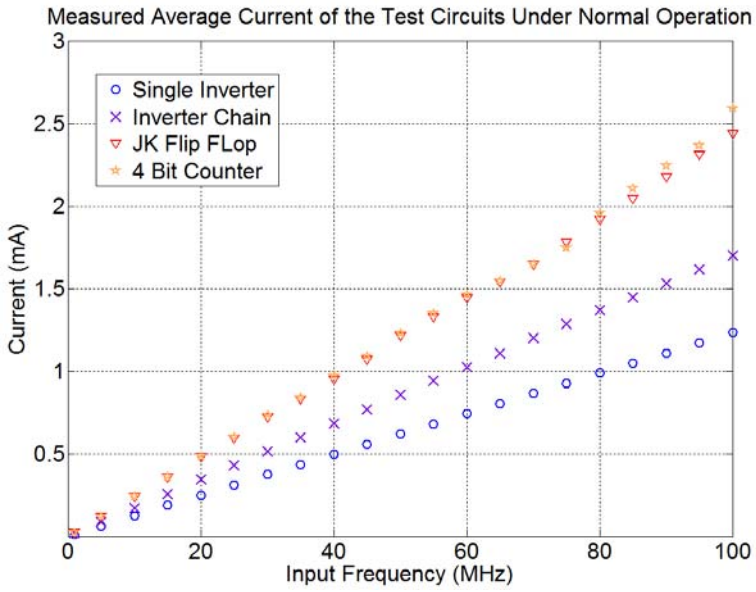

Figure 2.22: Average current measurement results for the HPM effects test circuits

The current of the test circuits increases linearly with frequency, which is consistent with basic circuit theory [44, 45]. Average current values for frequencies above 100 MHz can be linearly extrapolated from these results. Table 2.6 is the summary of the measurement results for the propagation delay and maximum average current for the full test circuits.

Table 2.6: Results of performance measurements for the test circuits under digital excitation

Circuit	*Propagation Delay (ns)*	*Maximum Frequency (MHz)*	*Average Current at maximum frequency (mA)*
Single Inverter	1.67	592 MHz	5.5
Inverter Chain	2.90	340 MHz	5.6
JK Flip Flop	6.92	140 MHz	3.2
4 Bit Counter	7.10	140 MHz	3.2

The results in table 2.6 will serve as a benchmark for comparison with the voltage and current characteristics measured in the HPM experiments.

Chapter 3 : Experimental Approach

3.1 Introduction

This chapter provides a detailed description of the experimental method developed to evaluate HPM effects in the test circuit. The objective of the experimental work is to characterize HPM signal transfer characteristics of the test circuits at the circuit terminals in order to determine the primary mechanisms of HPM effects and to facilitate the development of effects models. A great deal of importance is placed on precisely knowing input terminal voltages with respect to the observed output behavior. Great care is taken in all experimental measurements to minimize and account for the inevitable parasitic impedances introduced when taking measurements. Direct injection of HPM signals to circuit terminal and board traces are used to minimize any ambiguities in determining the terminal voltages, and provide an accurate means of controlling test parameters. Similar methods have been employed in many previous experiments used to study EMI effects and HPM effects [29, 30, 38, 42, 50].

3.2 Direct Injection Experiments

A schematic of the experimental setup for direct injection measurements is shown in Figure 3.1.

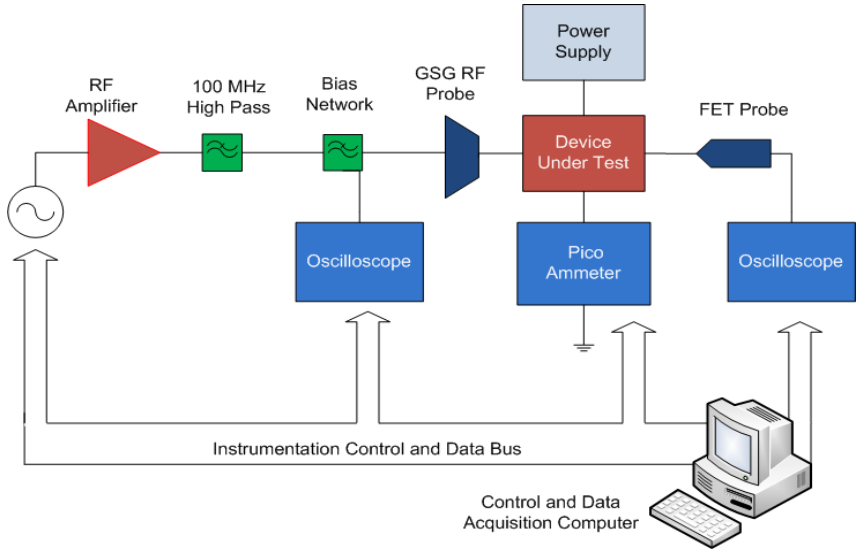

Figure 3.1: Schematic of the experimental setup for direct injection experiments

The signal generator used to create an HPM signal in the experiments is an Agilent E8257 D analog signal generator. The generator is capable of producing signals with frequencies ranging from 250 kHz to 40 GHz with various modulation schemes. To increase the power output capability of the test signal, the signal generator is fed into one of two RF amplifiers. Two different model amplifiers are used to cover the entire test frequency range. An OPHIR model 5303065 amplifier with a gain of 34 dB was used for the frequency range of 100 MHz to 1 GHz, and OPHIR model 5303053 with a gain of 31 dB was used for frequencies from 1 GHz up to 4 GHz. Each amplifier has a gain variation of +/- 2 dB. A 20 dB attenuator was connected between the signal generator and the amplifiers. This was done to decrease the sensitivity of the total output power to very small adjustments of the signal

generators output power. The output of the amplifier is attach to a 100 MHz high pass filter, which is meant to block any spurious DC bias from the amplifier from feeding to the input of the circuit.

The bias network is an arrangement of resistors chosen such that the input signal could be sampled while at the same time preventing the measurement probe from loading the RF input signal. A schematic of the biasing network is given in figure 3.2.

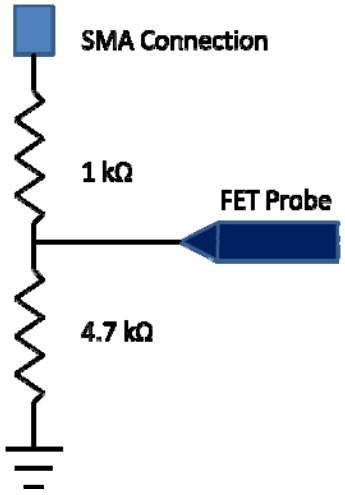

Figure 3.2: Schematic of bias network for probing input signals

The network is put together on a printed circuit board with surface mount resistors, and the traces made as short as possible to minimize any parasitic effects. The connection to the input is made through an SMA terminal attach to a T junction, which is in the main signal line. The ground connection is made to a metal plane on the printed circuit board. The probe attaches to the network via pins soldered directly to the board to minimize parasitic inductance. This method of probing the input was chosen so that information such as frequency content could be acquired at the input terminal along with input DC values. The traditional method is use to a commercial

bias T network; however, these devices only allow for DC measurements. The resistor creates a voltage divider with the measurement probe that needs to be accounted for to obtain accurate voltage information.

The bias network is connected to a Cascade Microtech FPC - 1000 ground signal ground (GSG) probe, which injects the RF signal into the DUT. The probe is mounted on a micrometer controlled precision positioner. Using a probe such as this offers several advantages over standard SMA connection. From a mechanical perspective, the probe easily positioned to various inputs of a test board. Also, the probes are very well matched to 50 Ωs and have impedance standards for calibrating a vector network analyzer for S-parameter measurements of board trace elements. A picture of the high pass filter bias network and RF probe is shown in figure 3.3.

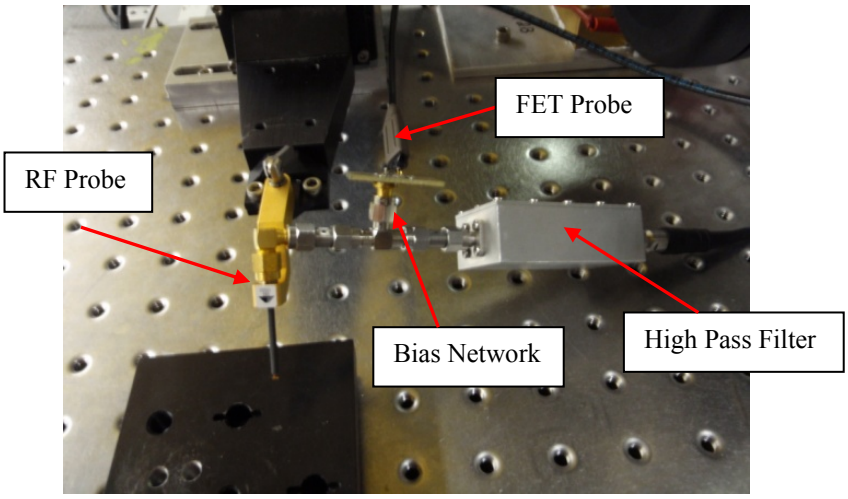

Figure 3.3: Photograph of the RF probe, bias network, and high pass filter

The probe positioner is attached to a 2.5' X 2.5' optical breadboard that serves as a mounting platform for the device under test (DUT) and any probe components. The DUT is mounted on a level plane that is attached to a micrometer positioner that allows for adjustments in the x, y, and z planes. A Zeiss Stemi 2000-C Stereo

Microscope is positioned above the platform and is used primarily for probe positioning. Figure 3.4 is a photograph of the breadboard mounting platform. The platform is easily configured to also accommodate on silicon probing, DC probing and device characterization, and 2 port VNA measurements using RF probes.

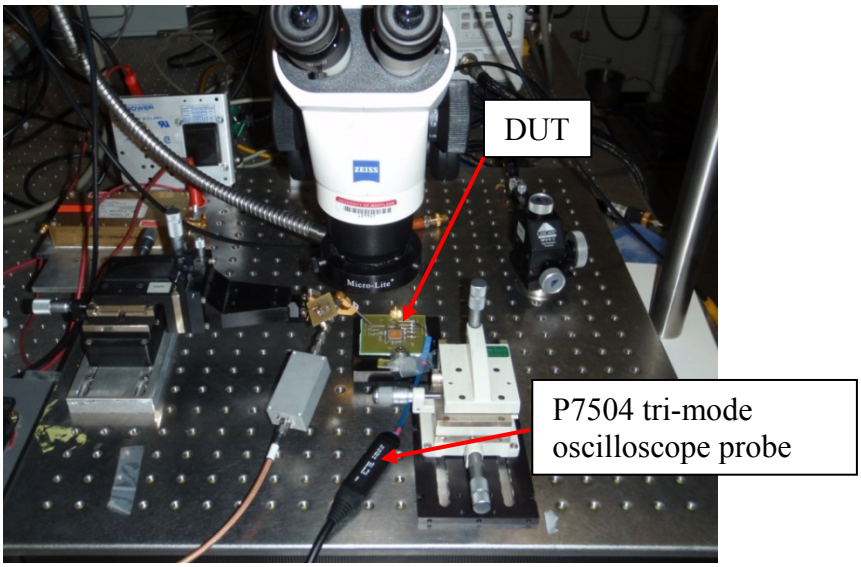

Figure 3.4: Photographs of the breadboard probing station

Three power supply units are mounted near the probe station to provide power to the two amplifiers and the DUT. A Keithley model 6487 picoammeter is connected to the power supply through the current return path of the DUT for current measurements. The picoammeter is capable of measuring average currents as small as 2 nA. There are two FET oscilloscope probes used to take measurements on the output, and the input though the bias network. The two probes available are the Tektronix P7240 active probe and the Tektronix P7504 tri-mode probe. Both probes introduce a load capacitance of approximately 0.9 pF and have a measurement bandwidth of 4 GHz. The P7240 is connected to the bias network and used to measure the input signal. The P7504 is provided with connections that are made to

solder directly to the measurement point on a printed circuit board. The solder connections are designed to keep the probe head as close as possible to the measuring point while greatly reducing any excess parasitic inductance introduced to the circuit. The P7504 probe can be seen in the photographs in figure 3.4.

The probes feed buffered signals to the inputs of a Tektronix model DPO 71254 digital oscilloscope for time domain signal measurements. The oscilloscope is capable of sample rates up 50 G/s. A photograph of the entire experimental apparatus is shown in figure 3.5.

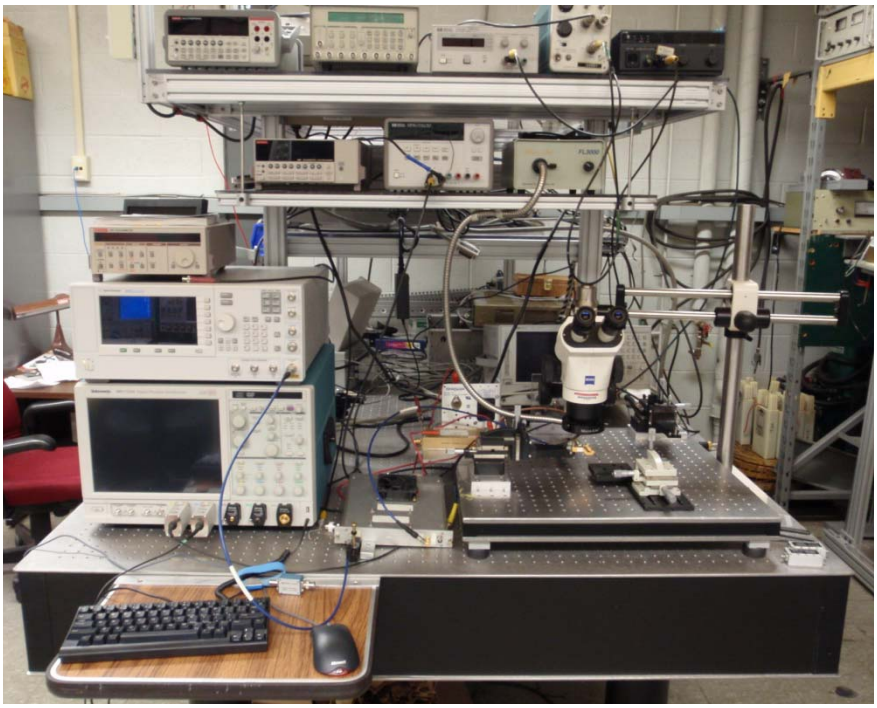

Figure 3.5: Photograph of the complete experimental setup

3.3 Printed Circuit Board Design

The printed circuits boards (PCBs) used to mount the test IC's were custom designed using the commercial software PCB Artist. The design philosophy for the PCBs is to create realistic circuit boards designed as if the test circuit were going to

be used under normal operating conditions. This is done to incorporate realistic parasitic elements into the test measurements in order to account for their contribution to HPM effects.

The board itself is standard FR4 with copper metal layers. The PCBs were laid out using common design conventions. One important convention is the use of a metal layer as the ground plane. All ground connections to the test chip occur through vias to a metal backplane to eliminate the problem of ground bounce, especially at frequencies above 1 GHz. The power connection to the circuit is made through a short trace from a SMA connection. A surface-mount capacitor is connected between the power trace and ground through a via located very close to the power pin connection on the chip. This is a local by-pass capacitor that provides transient current to the circuit during a change in state. The value of the capacitance used on all the test circuits is 0.1 μF.

The signal traces are 0.6 mm wide and trace lengths range from 1 cm to 3 cm. At the end of each trace is a GSG probe pad with a 1 mm pitch to match the Cascade RF probes. The input traces also have a surface mount 10 kΩ pull down resistor attached in parallel to prevent an input that is not being probed from floating. The traces themselves are not designed to be match to 50 Ω. When the circuit is operating at normal frequencies, the wavelength is many times the length of the circuit traces and matching is not required. A photograph of a test board is shown in figure 3.6.

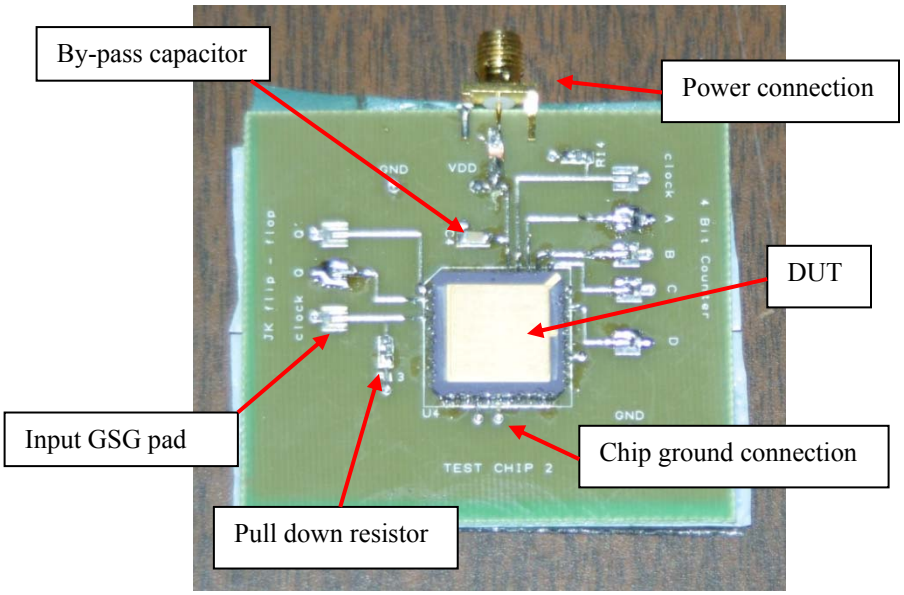

Figure 3.6: Photograph of a test PCB design for a chip containing the JK flip flop and the 4 bit counter

Throughout the entire test setup, great care was taken to eliminate and minimize any impedance introduced to the measurements by the apparatus. One of the greatest areas of concern was the power leads from the power supply to the DUT. The by-pass capacitor should eliminate much of this concern; however, to ensure measurements were not overly influenced by these impedances, a battery attachment was made for use on the DUT. No current measurements could be made with this attachment, so the battery was used as a means to verify that the input and output behavior is a result of legitimate circuit dynamics and not caused by unrealistic power line impedances. A photograph of the battery attachment is shown in figure 3.7.

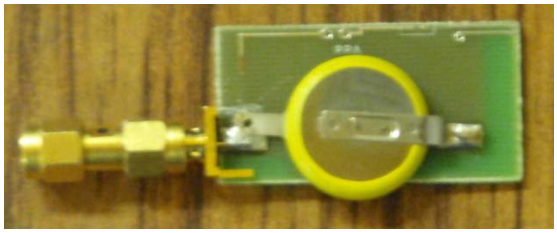

Figure 3.7: Battery attachment for the DUT

3.4 Experimental Methods

3.4.1 Instrument Control and Data Acquisition

All of the electronic instruments described above are connect to a central control computer through a GPIB bus. The front panel control of each instrument was managed using Agilent VEE pro software. VEE pro is a graphical based programming language intended for external instrument control. Functional blocks that serve specific tasks such as a loop counter, instrument control, or output display are connected to each other through flow control and data wires. The routine is designed by attaching the appropriate wires to the terminals of each of these blocks in order to perform a desired task. The basic programming blocks are essentially visual forms of common programming languages such as C and C++. Instrument control blocks communicate though the GPIB bus using the command language specific to that instrument. An example VEE program is shown in figure 3.8. The VEE programs control the flow of the experimental measurements by incrementing frequency and output power, recording data from the instruments, and saving data to comma-delimited text files.

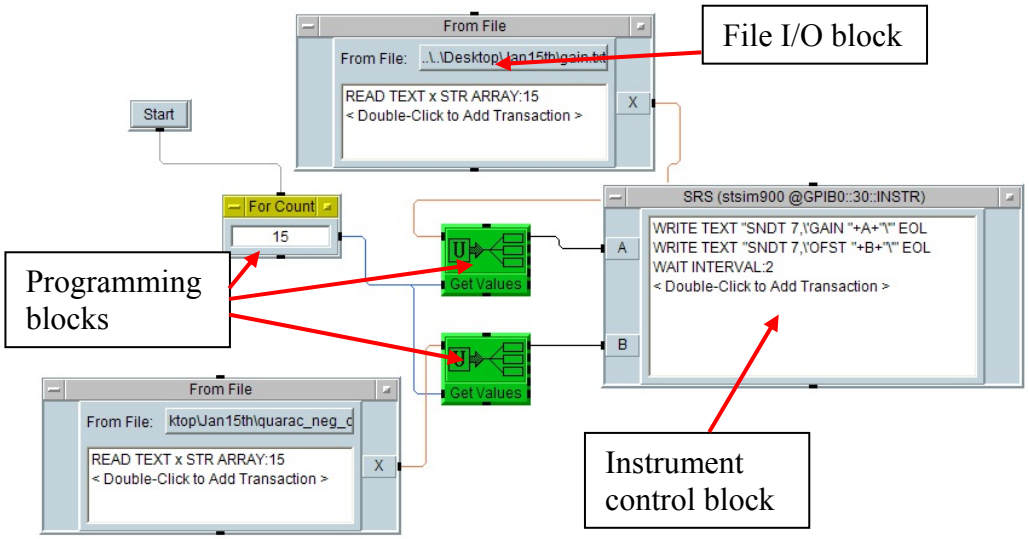

Figure 3.8: Example program written in Agilent VEE Pro.

3.4.2 Measurement Procedure

This sub-section describes the experimental measurement procedure used for the vast majority of data presented in this work. The experimental measurements begin with the injection signal generated by the RF source, which is directed into the test circuit input trace. A pulsed modulated signal is always used to prevent thermal effects in the DUT. The modulation pulse width was typically set between 3 and 10 μs and the repetition period was 100 μs to keep the duty factor low. The carrier frequency and power were stepped in increments of 5 MHz and 0.5 dBm from 0.1 GHz to 4 GHz and -20 to 20 dBm, respectively, and the digitized waveforms were recorded at each drive setting. The typical frequency increments were as follows: 100 MHz, 200 MHz, 400 MHz, 600 MHz, and 800 MHz on the low frequency amplifier and 1 GHz to 4 GHz in steps of 500 MHz on the high frequency amplifier. The experimental range was chosen based on observations made in previous HPM studies [5, 38, 40, 42].

The pulse modulation envelope is fed out to synchronize both the oscilloscope and the picoammeter. The picoammeter was triggered so that the current measurement coincided with the injected RF pulse. The instrument can be set to integrate an integer multiple or a fraction of a power line cycle period (~16 ms). An appropriate line cycle fraction was chosen to integrate over as much of the RF pulse as possible. The oscilloscope recorded input and output voltage waveforms for each power and frequency setting for a given experiment. The sample rate was set to 25 Gs/s in order to record some of the higher harmonics generated by nonlinear effects in the circuits. The data was written to a text file along with the appropriate frequency and output power information. Record lengths of the waveforms were typically 200000 points.

Chapter 4 : Input Analysis and ESD-HPM Interaction

4.1 Introduction

The following chapter presents experimental measurements performed to characterize the nonlinear response of ESD protection devices when excited by large voltage amplitudes associated with HPM signals. How ESD circuits respond to high-frequency large-signal excitation is an important aspect of HPM effects, since they are found in virtually all modern integrated circuits. When HPM signals interact with the ESD devices the primary effect observed is an increase in the average DC voltage level at the input [42]. The shift in the DC voltage at the input of the CMOS test circuits on its own has been shown to be a source of logical bit errors depending on whether or not the severity of the DC shift rises above the noise margin[42]. However, the response of these devices may also be responsible for other effects observed in commercial devices [38]. If these and a host of other complex effects are just consequences of ESD response then circuit models and simulations can be formulated based on a simple mechanism.

4.2 Theoretical Background – PN Junction Transient Analysis

The primary device of interest in the ESD protection circuits is the diode created by the drain body PN junction of the gate grounded (ggNMOS) and the gate grounded (ggPMOS), which is shown in Figure 4.1.

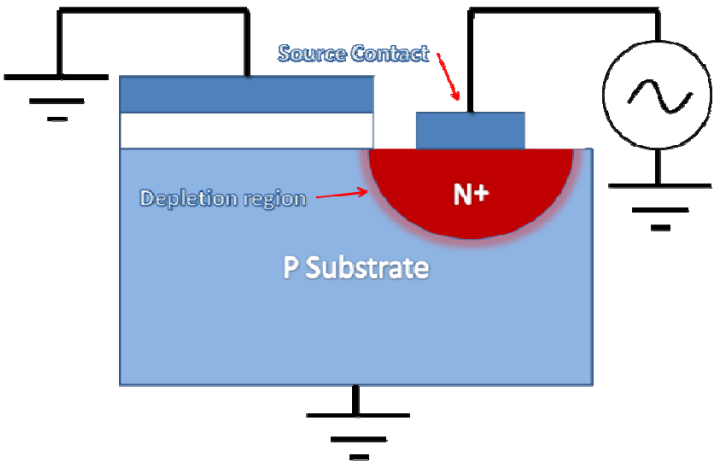

Figure 4.1: Drain body PN junction for a ggNMOS

To develop an understanding of how the diode behaves when excited by large signals it is important to evaluate how the PN junction behaves as the terminal voltage swings from a forward bias condition to a reverse bias condition. The quasi-static approximation for a diode assumes that the carriers within the junction redistribute in a time that is short compared to transients in applied voltage [51]. In other words, the approximation assumes that the junction potential follows the applied voltage perfectly as the applied voltage transitions from forward to reverse bias levels. Under these conditions a sinusoidal waveform produces an ideal half wave rectified voltage drop across the diode junction.

If the applied voltage transitions very rapidly from forward to reverse bias, the quasi-static approximation begins to break down and the time it takes for the junction voltage to reach steady state reverse bias must be considered. This is referred to as non-quasistatic (NQS) regime of operation and the transition from forward bias to reverse bias is referred to as the reverse recovery time [51-53]. For the case of high frequency sinusoidal excitations under NQS conditions, the signal is not rectified in the ideal sense as described above. However, as with any nonlinear circuit element, a

DC component will continue to be generated until the frequency is high enough that the change in junction voltage from its forward bias state is negligible.

Useful insight into the operation of the drain body diode under large signal high frequency excitation can be developed from theory by using some of the typical analytical approximations established by the basic semiconductor physics. The following analysis will focus on the dynamics of the transient response of the PN junction as the applied voltage shifts abruptly from forward bias to reverse bias.

4.2.1 Linear Approximations and Initial Steady State

The dynamic behavior of the PN junction is best understood in terms of the minority carrier concentrations and how those concentrations change versus time as a junction is driven from forward bias to reverse bias. In forward bias, either side of the PN junction is flooded with minority carriers and the diffusion of minority carriers at the junction boundary accounts for the forward bias diode current. For the purpose of this analysis, it is sufficient to assume a planar abrupt PN junction. Under this assumption the depletion region is devoid of any mobile carriers and consists only of fixed ion charges. This is often referred to as the depletion approximation[51-53].

Consider the ggNMOS device shown in figure 4.1. In the process technology used for the test circuits created for this study, the n+ source region is degeneratively doped with impurity concentrations on the order N_d ~ 10^{20} per cm^3 and the p-type bulk has a doping concentration of approximately N_a ~ 10^{16} per cm^3 [43]. As a result the conductivity of the n+ region is much great than the p-type substrate. Therefore, for the case of forward bias, the minority carrier concentration in the n+ region is negligible and the depletion region is located almost entirely in the p-type bulk

region. The minority carriers in the n+ region can be neglected, which simplifies the analysis. The source ground contact for the ggNMOS is 0.9μm and is much shorter than the diffusion length of minority electrons in the p-type bulk, which is on the order of 10μm [52]. Since the ground contact is such a short distance from the PN junction, it is appropriate to apply the short-base diode approximation. The excess minority electron concentration in the steady state forward bias condition for a short base diode is described by equation (4.1) [52].

$$n_p(x) = n_{p0}(e^{\frac{qV_a}{kT}} - 1)(1 - \frac{x + x_p}{W_B}) \tag{4.1}$$

where W_B is the distance from the junction boundary to the source contact, k is the Boltzmann constant, T is the temperature in Kelvin, x_p is the location of the depletion region edge with respect the junction boundary, φ_i is the built in potential of the junction, V_a is the applied voltage, and n_{p0} is the steady zero bias minority carrier concentration defined as,

$$n_{p0} = N_d e^{\frac{-q\phi_i}{kT}} \tag{4.2}$$

The current at the junction boundary is entirely due to minority carrier diffusion. Since the minority carrier concentration in the n+ region is neglected, the total current density for steady state forward bias can be calculated by solving the steady state diffusion equation (eq. 4.3) at the depletion boundary, with the minority carrier concentration at the boundary described by equation (4.4) [51-53].

$$J_t = -qD_n \frac{dn_p(x)}{dx}\Big|_{x=0} \tag{4.3}$$

$$n_p(0) = n_{p0}(e^{\frac{qV_a}{kT}} - 1) \tag{4.4}$$

Figure 2 shows the single-sided junction and illustrates the minority carrier concentration of the p-type region in steady state forward bias.

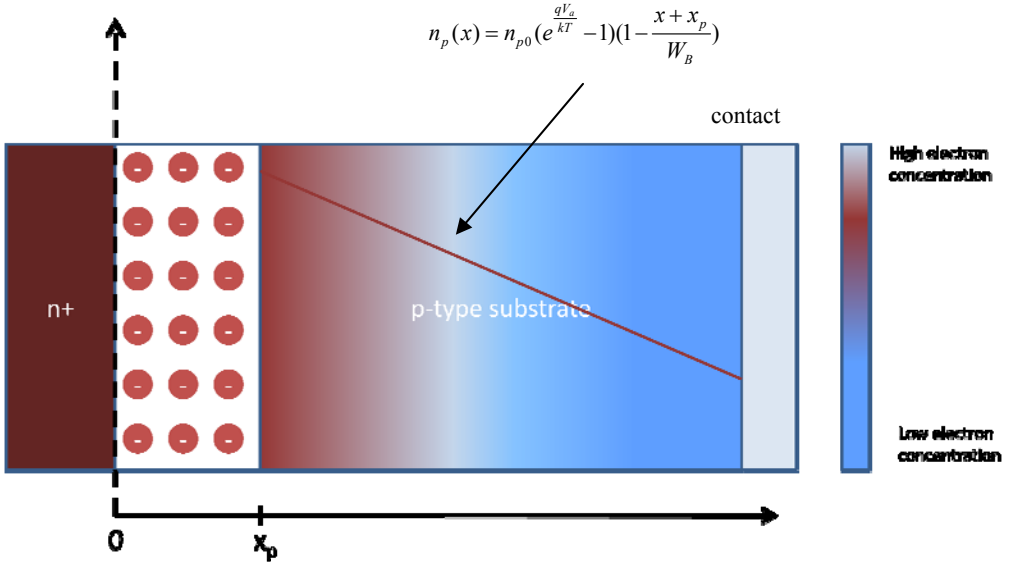

Figure 4.2: One sided step junction in steady state forward bias

The reverse bias condition of a PN junction occurs when the voltage drop across the depletion region is nearly equal to the applied voltage. Under these conditions, the depletion region expands, the concentration of excess minority carriers drastically decreases, and almost no current flows though the diode (there is always a degree of reverse current due to generation in the depletion region but this is ignored under the depletion approximation) [51-53]. This is in contrast to the forward bias condition, in which very little voltage is dropped across the depletion region and there is, relatively speaking, a large amount of excess minority carriers. The change in minority carriers does not happen instantaneously and evaluating the transient behavior of the minority carriers is the key to understanding the reverse recovery process.

4.2.2 Reverse Recovery Transient

Once the applied voltage switches to from forward bias to reverse bias the excess minority carriers transit away from the junction boundary until they recombine and are effectively removed from the bulk. The time it takes for the excess carriers to recombine can be broken into two phases. During the first phase, excess minority carriers at the junction boundary maintain the gradient necessary to allow current to flow through the device. Immediately after switching, a reverse current will flow through the diode limited only by the impedance of the external circuit. This current will flow until the all the excess minority carriers have diffused away from the junction boundary. During this period the junction voltage changes by a very small amount. This phase is commonly referred to as the storage phase.

The second phase is defined by the time needed to evacuate the remainder of the stored excess minority carriers. During this phase the reverse current will decay because the minority carrier gradient at the boundary is no longer present to maintain the reverse current. As the current decays the junction potential approaches the applied bias potential until the steady state reverse bias is reached. Figure 4.3 illustrates the behavior of the reverse current versus time. The length of time that defines the second phase or recovery phase is determined by the point at which the reverse current reaches 10% of its initial value. The reverse recovery time is defined as $t_{rr} = t1 + t2$.

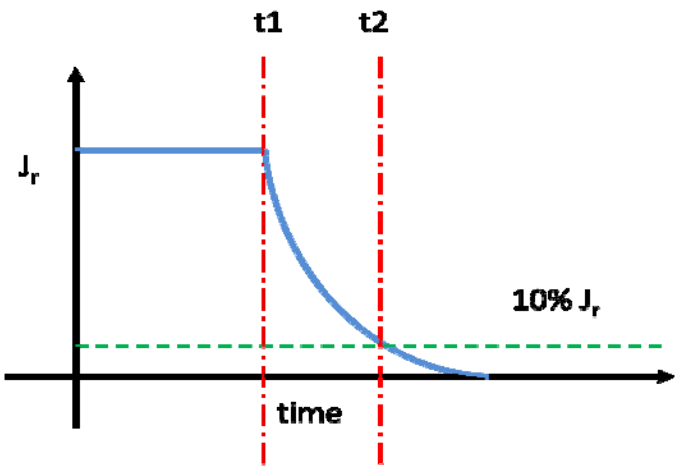

Figure 4.3: Reverse current vs time. *t1* is the length of time for the storage phase and *t2* is the time of the recovery phase defined by the point at which the reverse current reaches 10% of its initial value.

The junction potential during the reverse recovery process is defined by the following expressions:

- $t = 0$ $$V_{junction} = V_{fb} \quad (4.5)$$
- $0 < t < t1$ $$V_{junction} = \frac{kT}{q} \ln \frac{n_p(0,t)}{n_{p0}} \quad (4.6)$$
- $t \approx t1$ $$\frac{kT}{q} \ll V_{junction} < V_{bias} \quad (4.7)$$
- $t1 < t < t2$ $$V_{junction} = V_{bias} - RI_{reverse} \quad (4.8)$$
- $t \gg t2$ $$V_{junction} = V_{bias} \quad (4.9)$$

Equation (4.6) shows that during the storage phase the potential changes as the minority carrier concentration changes with time, but the junction potential will remain on the order of *kT/q*. During the recovery phase described by equation (4.8), the junction voltage will steadily increase as the reverse current decays. The voltage due to the reverse current is determined by the internal resistance and external impedance present in the actual circuit.

For a large signal sinusoidal excitation of the diode, the consequence of the reverse recovery process becomes more pronounced as half the period of the sine wave becomes comparable to the reverse recovery time. The average DC voltage of the reverse bias half of the sinusoidal will be reduced by the transient response of the junction voltage, which defines the frequency dependence of the rectification efficiency of ESD protection circuit.

4.2.3 Approximation of Non-Quasi-static Effects

In order to analytically determine the reverse recovery time and the corresponding time dependent junction voltage, one must solve the time dependent diffusion equation given by equation (4.10).

$$\frac{\partial n_p(x,t)}{\partial t} = D_n \frac{\partial^2 n_p(x,t)}{\partial x^2} + \frac{n_p(x,t) - n_{p0}}{\tau_n} \tag{4.10}$$

The solution to the time dependent diffusion equation, using the same approximations defined in section 4.2.1, has been presented by many authors [51, 54-56]. Each of the authors take the same general approach of breaking the problem into the two phases described in the previous section, and by defining the respective boundary conditions for each phase. The mathematical analysis in [54-56] too lengthy to be presented here, but the results of the analysis can be used to obtain a good approximation of the reverse recovery time of the ESD protection devices and the DC response of the devices versus excitation frequency.

In [55], Kingston presents the analytical solutions to the time dependant diffusion equation for a short base diode. This solution is the most applicable to the ESD protection devices because the distance from the drain body PN to the source is

much shorter than the diffusion length. Kingston uses his solution to calculate the reverse recovery time as a function of minority carrier lifetime and the ratio of forward bias current to the initial reverse current. Assuming a current ratio I_r/I_f =1, Kingston's results show that the reverse recovery time is approximately 0.5τ, where τ is the minority carrier lifetime [55].

Another approach to estimate the reverse recovery time is to make some further approximations to simplify the analysis. One way to simplify the solution is consider the total minority carrier charge as a lumped charge Q instead of considering the minority carrier distribution as a function of position. The total charge is then a time-dependent function of the reverse current described by the solution of equation 4.11.

$$I_r(t) = \frac{Q(t)}{\tau} + \frac{dQ(t)}{dt} \quad , \quad Q(0) = I_f \tau \tag{4.11}$$

The solutions to this equation yields equation (4.12), which when solved for t when Q(t) = 0 yields equations (4.13).

$$Q(t) = \tau[-I_r + (I_f + I_r)e^{\frac{-t}{\tau}}] \tag{4.12}$$

$$t_{rr} = \tau \ln(1 + \frac{I_f}{I_r}) \tag{4.13}$$

This approximation estimates the reverse recovery time by relating the time it takes for all of the excess minority carrier charge to recombine with respect to the recombination rate. The approximation does not account for the spatial distribution of excess minority carriers and the resulting current density like the more exact

treatment of Kingston. Assuming a current ratio of I_f/I_r=1 equation (4.13) yields a reverse recovery time of 0.69τ.

The minority carrier recombination lifetime of both electrons and holes in silicon is very long compared to the time it takes for the minority carriers to diffuse away from the drain body junction region and reach the source. An effective lifetime can be calculated from equation 4.14.

$$\tau_{eff} = \frac{L_{eff}^{\ 2}}{D_{n,p}} \tag{4.14}$$

In equation (4.14), the effective length, L_{eff}, is the distance from the drain body PN junction to the source, which for the ESD protection devices is 0.9 μm. $D_{n,p}$ is the diffusion constant for electrons and holes respectively. The diffusion constant is defined by equation (4.15) where $\mu_{n,p}$, is the mobility of electrons or holes in silicon respectively.

$$D_{n,p} = \frac{kT}{q}\mu_{n,p} \tag{4.15}$$

The common values of $D_{n,p}$ for holes and electrons in silicon and the calculated effective minority carrier lifetime are given in table 4.1.

Table 4.1: Minority carrier diffusion constants in silicon

Minority Carrier	*Diffusion Constant (cm^2s^{-1})*	τ_{eff} *(ps)*
Electrons	34.6	234
Holes	12.3	658

Using the reverse recovery time estimation derived from the previous analysis, approximations can be used to predict the DC diode response versus

frequency for the ESD protection circuits. The approximation in the following analysis is that the junction potential remains at the forward bias level for the duration of the reverse recovery process as shown in figure 4.5. This approximation ignores the steady increase of the junction potential as the minority carrier distribution changes, especially during the recovery phase. However, the approximation is suitable for evaluating the diode response over a broad range of frequencies. Consider the reverse bias half sine wave voltage in Figure 4.4.

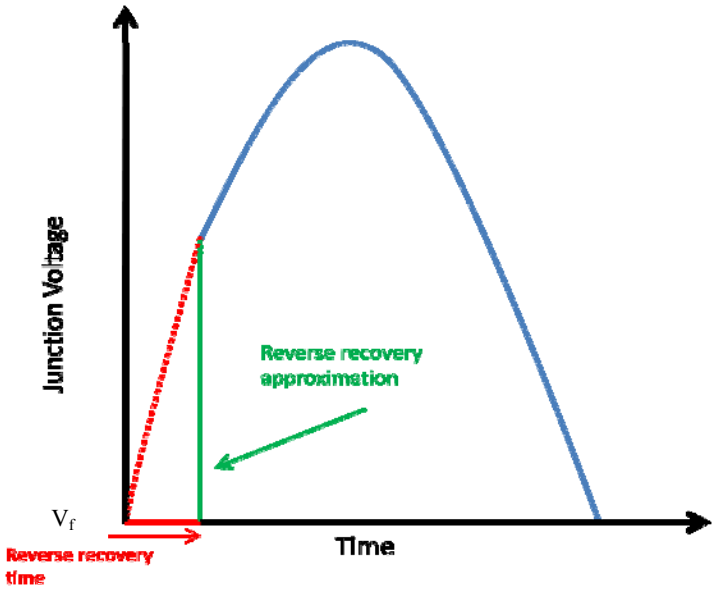

Figure 4.4: The effect of the reverse recovery approximation

As frequency increases, the reverse recovery time becomes more comparable to the reverse bias period of the sinusoidal signal and the DC average voltage is reduced. Using the calculated reverse recovery times presented in table 4.1, the DC response for of a sinusoidal excitation with a 1 V amplitude and a frequency range from 100 MHz to 10 GHz was calculated with the results shown in figure 4.5.

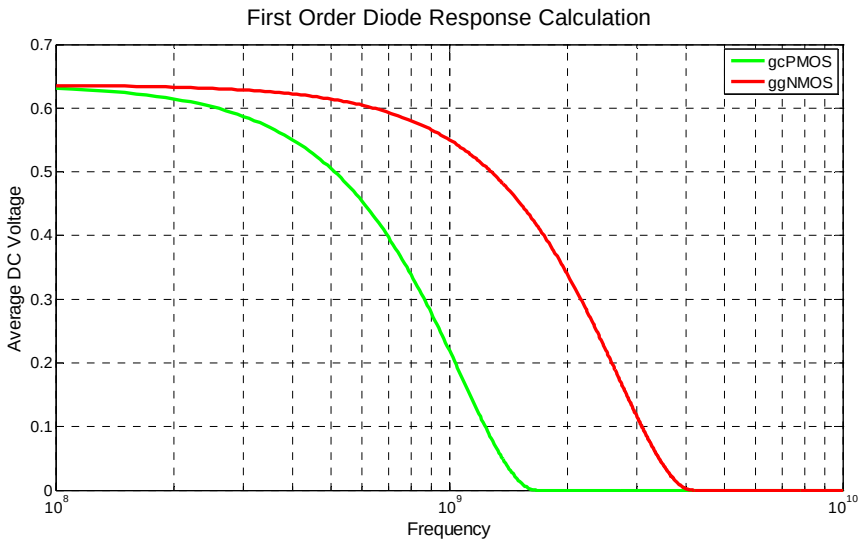

Figure 4.5: Calculated ESD protection device DC response over a frequency range of 100 MHz to 10 GHz

An interesting result from the calculation is that the response of the ggPMOS falls off more quickly than the ggNMOS. This is caused by the difference in the mobility of minority carriers for each device. The minority carrier of the n-type body of ggPMOS is the hole. The mobility of the holes in silicon is approximately one third of the mobility of electrons [52], which accounts for the difference in the diffusion constants in Table 4.1.

In order put into perspective the consequence of the difference in DC response of the ggPMOS and the ggNMOS, consider the simplified input circuit in Figure 4.6.

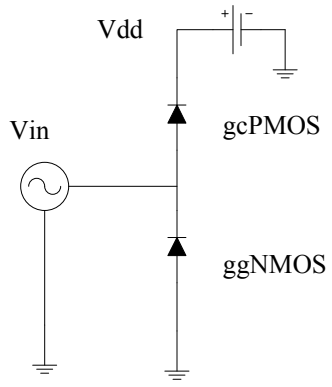

Figure 4.6: Simplified schematic of input ESD protection device arrangement

As the amplitude of Vin increases beyond the diode turn on voltage, the ggNMOS will begin to rectify the signal. The DC average will continue to increase as the amplitude of Vin approaches V_{dd}. Once the amplitude of Vin exceeds V_{dd} by the diode turn on voltage, the ggPMOS will start to rectify and offset the DC response of the ggNMOS. The average DC voltage under the ideal diode/quasi static condition will not exceed $V_{dd}/2$. At high frequencies such as 1 GHz, the rectification efficiency of the gcPMOS is less than that of the ggNMOS. Under such conditions the average DC voltage will continue to rise beyond $V_{dd}/2$ even once the amplitude of Vin goes beyond V_{dd}.

In the context of HPM effects, the above theory and analysis predicts HPM signals that couple into input terminals will interact with the ESD circuits and cause a substantial DC bias shift to the input of the circuit. The level of the DC bias can be as high as V_{dd} depending on the frequency and the amount of power that couples to the circuit.

4.3 Experimental Results

The following section presents the results of the experimental measurements of the input stage of the tests circuits when excited by HPM. The experimental setup is for this measurement was discussed in detail in chapter 3. The input stage of each test circuit has the same generic topology, which is illustrated in figure 4.7.

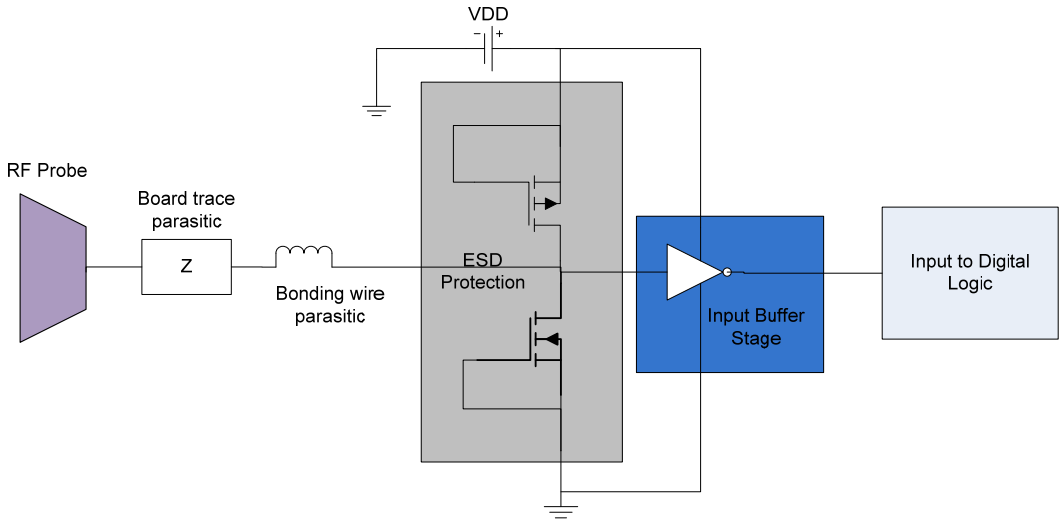

Figure 4.7: Test circuit input stage measurement schematic

The measurements were taken with the output of the signal generator, before amplification, ranging from 5 mV to 400 mV in steps of 5 mV when using the low frequency amplifier (100 MHz to 900 MHz). When using the high frequency amplifier (1GHz to 4 GHz), the signal generator output ranged from 10 mV to 800 mV in steps of 10 mV. The total RF power after amplification for both amplifiers ranged from -20 dBm to 20 dBm. The frequency was varied from 100 MHz to 4GHz in steps of 100 MHz. The detected voltage at the test circuit input was recorded for each step in amplitude for each frequency. The detected voltage in this dissertation

will refer to the time averaged voltage measurement at the circuit input. An example of detected voltage measurement on an input waveform is shown in Figure 4.8.

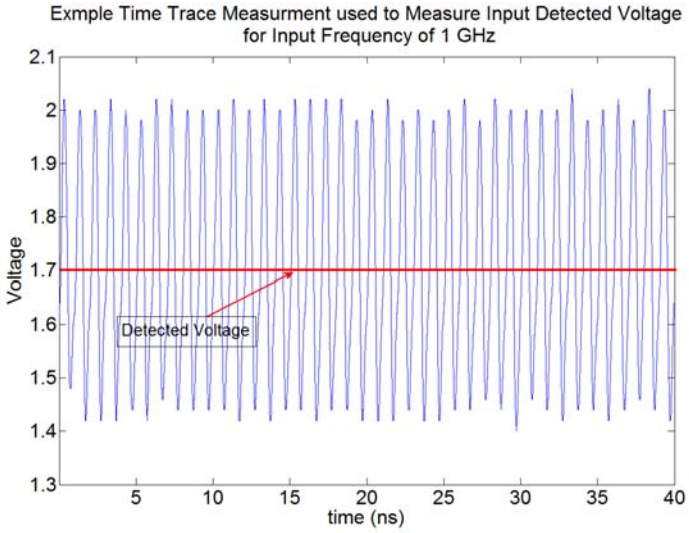

Figure 4.8: Example time trace illustrating how detected voltage is measured.

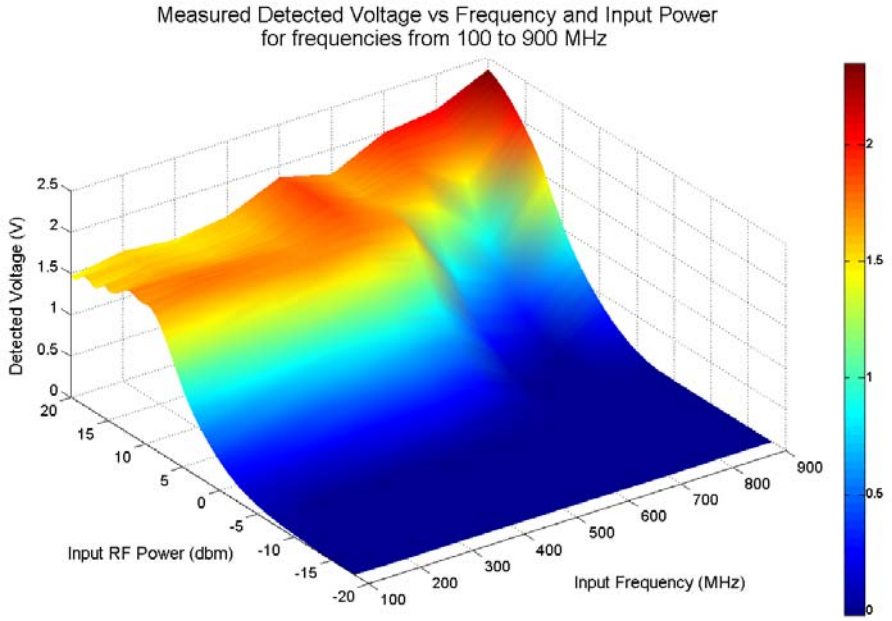

Figure 4.9: Measured Input detected voltage for frequencies 100 MHz to 900 MHz, which illustrates how ESD diode response changes with frequency.

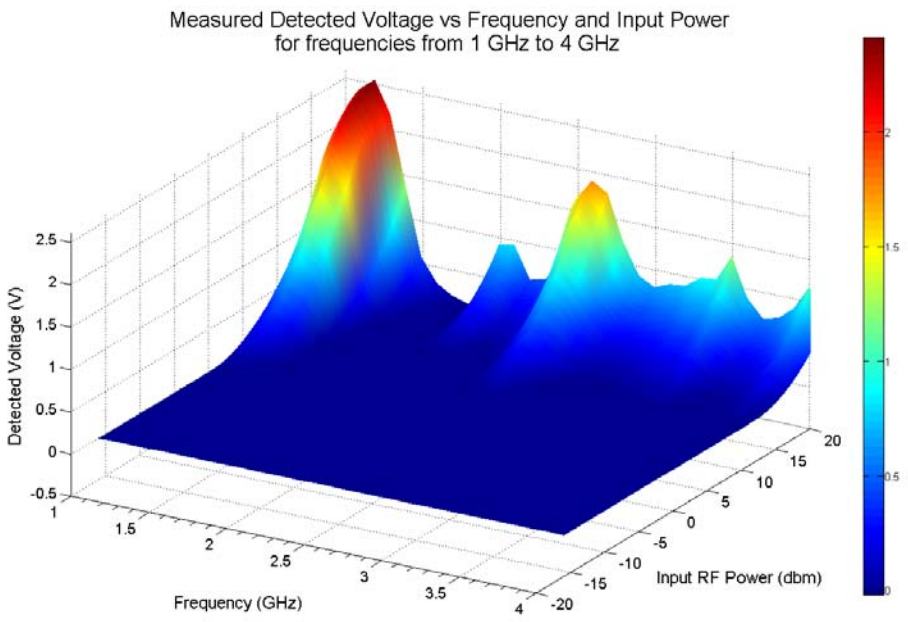

Figure 4.10: Measured Input detected voltage for frequencies 1 GHz to 4 GHz, which illustrates how ESD diode response changes with frequency.

Figures 4.9 and 4.10 are plots of the results. The shading between 100 MHz steps in the plots is the result of linear interpolation between frequency data sets. The 3D plots present a good overview of the DC response of the input stage and highlight several important results. One of the most noticeable aspects of the results is the occurrence of the peaks and valleys in the measured detected voltage, especially at higher frequencies.

4.3.2 Accounting for linear parasitic elements

Linear parasitic elements can potentially create resonances, which may also influence the input response. The parasitic impedances are linear impedances setup by ball bond wires, lead frames, circuit board traces, and impedances introduced by the experimental apparatus. In order to interpret the measurement result in terms of the ESD response to HPM signals, the variation of response attributed to the linear

parasitic elements needs to be understood. Therefore measurement of linear parasitic elements is a critical component of evaluating and eventually modeling HPM effects. Parasitic impedances are unavoidable and exist in every microelectronic system. The effects of these impedances become more pronounced as HPM wavelengths become more comparable to circuit traces, ball bond wires, etc.

Figure 4.11 is a combined cut of figures 4.9 and 4.10 at a fixed output power across the entire test frequency spectrum.

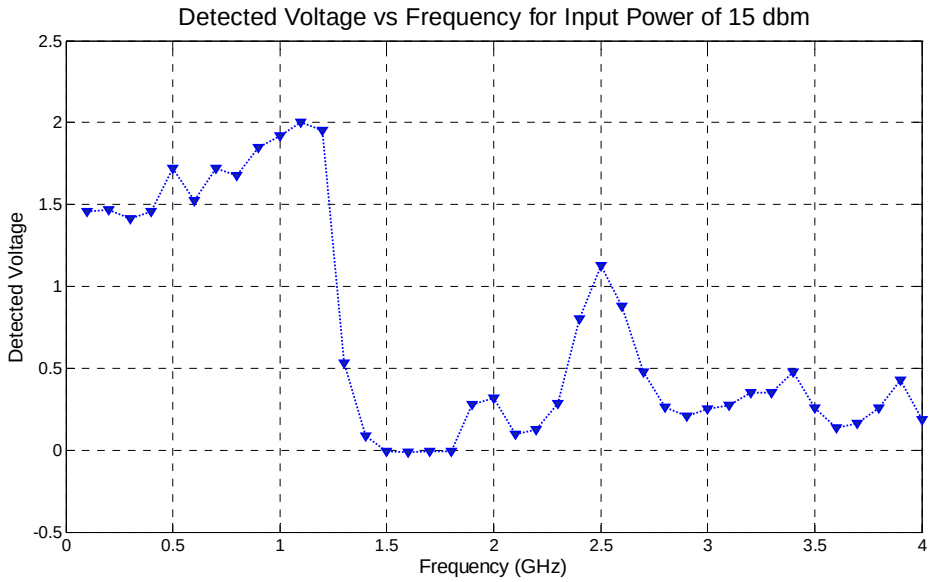

Figure 4.11: Detected voltage vs. frequency for a constant input power of 15dBm demonstrating the effects of linear parasitic elements on the input response.

The response shows multiple resonances at frequencies above 1.2 GHz. The most noticeable resonance occurs between 1.3 GHz and 2.3 GHz, which would suggest a very strong parasitic resonance within that frequency band. In order to determine the frequency response of the linear parasitic elements, a test board was created with the identical layout to the test chip printed circuit board. The test board is shown in figure 4.12

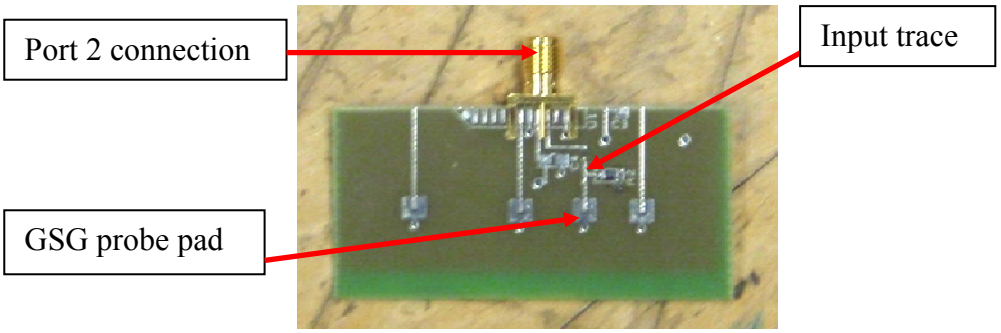

Figure 4.12: Input test board used to measure linear parasitic elements

An S-parameter measurement was performed on the test board over a frequency range of 100MHz to 4 GHz in order to characterize the frequency response of the parasitic elements. The experimental apparatus from the output of the amplifier up to and including the RF probe were included in the measurement to account for any parasitic elements introduced by the experimental setup as well. One important element not included in the measurement is the lead frame and ball bond wire, which primarily introduce an inductance on the order of 1 to 5 nH depending on the length of the ball bond wire [57].

The experimental setup for the S-parameter measurement is shown in figure 4.13. Each element is arranged in precisely same manner it is for the input detected voltage measurement.

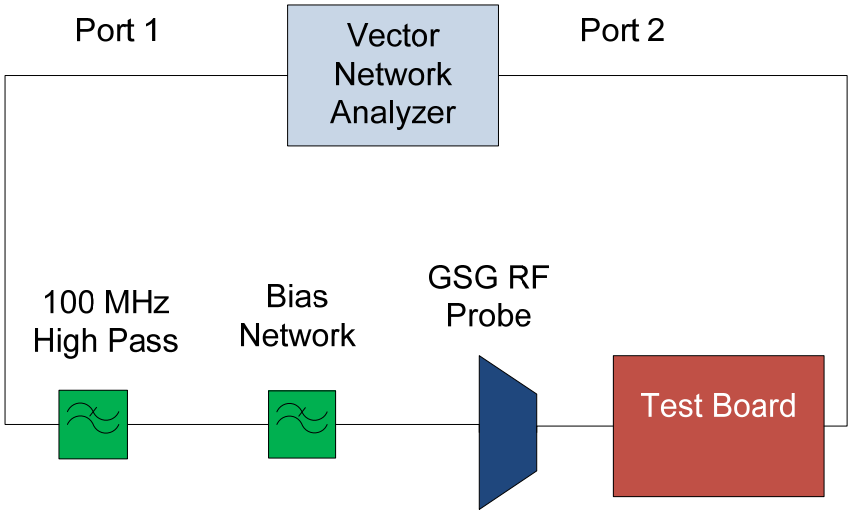

Figure 4.13: Test setup for measuring the S-parameters of the linear parasitic elements

Figure 4.14 shows the magnitude of the forward reflection coefficient, S11, and the forward transmission coefficient, S21, in dB. Figure 4.15 shows the same as figure 4.14 except for the reverse reflection and transmission coefficients, S22 and S21.

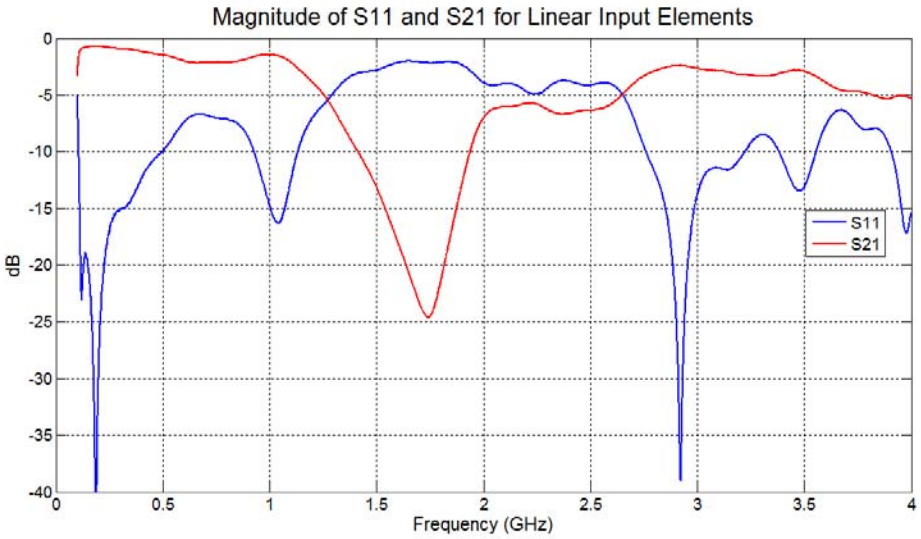

Figure 4.14: Forward reflection and transmission coefficients for the input linear parasitic elements.

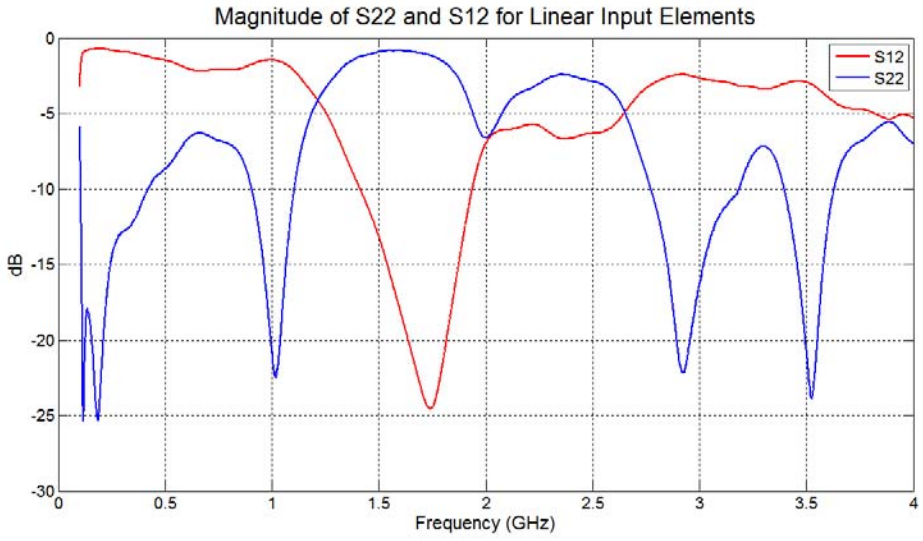

Figure 4.15: Reverse reflection and transmission coefficients for the input linear parasitic elements.

Notice the strong valley in the S21/S12 that peaks at about 1.7 GHz. The strong resonance in S21/S12 means that any input signal in the frequency range of approximately 1.4 GHz to 1.9 GHz will only transmit from 10 % to less than 1 % through to the circuit input. The result of this measurement confirms that the severe drop in response over the same frequency range shown in figure 4.11 is due entirely to the linear parasitic elements. This is also just one example of how important it is to account for parasitic elements as much as possible when dealing with high frequency HPM effects.

4.3.3 Determining the Voltage Amplitude at the Input

The ultimate goal in evaluating the linear parasitic elements is to properly determine the voltage at the ESD protection devices for each frequency and for a given input power. Besides the information about the response of the linear elements provided by the S-parameter analysis, there are two other important aspects to

account for in order to accurately determine the true voltage at the input pin of the test chip.

While the output power gain of the two RF amplifiers is known, calculating the voltage gain is not a simple task. The output impedance of the amplifiers is 50 Ω's, however beyond the RF probe there is certainly not a matched 50 Ω load. This situation is very realistic for a typical CMOS digital circuit. While precise high frequency RF analog devices require rigorous micro-strip design to match impedances, low frequency digital circuits require no such matching, and matching impedance for digital circuits that operate at the frequencies of the technology used in this study is not common practice. In the experimental measurement, there are several locations where impedance mismatches occur, such as where the RF probe contacts the GSG pad, the point where the lead frame is soldered to the trace, etc. These impedance mismatches will have a significant effect on the input voltage.

For a perfectly matched load, the voltage amplitude in the transmission line is constant. Mismatched impedances cause reflections in transmission lines. The reflected wave will constructively interfere with the forward wave creating periodic variations in the voltage magnitude along the transmission line referred to as standing waves. The magnitude of the voltage along a transmission is defined by equation (4.16) [58],

$$\left|V(z)\right| = \left|V_0^+\right|\left|1+\left|\Gamma\right|e^{j(\theta-2\beta z)}\right| \tag{4.16}$$

where $|V_0^+|$ is the magnitude of the forward wave, $|\Gamma|$ is the magnitude of the reflection coefficient, θ is the phase of the reflection coefficient, and z is the distance from the generator. β is defined by equation 4.17.

$$\beta = \omega\sqrt{\mu\varepsilon} \tag{4.17}$$

For a fixed value of z such as the distance to the load, equation (4.16) is a periodic function of frequency and therefore the voltage amplitude at a mismatched load is frequency dependent. The amplitude of the voltage at the load will vary from 0 to 2 times the input voltage amplitude. The extremes of 0 and 2 times $|V_0^+|$ only occur total reflection ($|\Gamma|=1$), which is a perfect open load or a short.

The second important consideration is the gain flatness of the amplifiers. Solid state amplifiers are not perfect and do have some variation in gain over their frequency band. As was mentioned in Chapter 3, both amplifiers have a gain variation of +/- 2dB.

Considering all the potential complexities in calculation the voltage the input pin of the test circuit, it was determined that the best and most accurate approach would be to measure the voltage gain across all the linear elements of the experimental setup. The experimental setup for this measurement is exactly the same as the setup used to measure the DC response of the ESD protection devices. The test board in figure 4.12 was used with the SMA connection replaced with a solder point for the FET probe. This allows the probe to be connected as close as possible to the board and reduces any addition parasitic impedance.

The FET probes have a capacitance of about 1 pF that they introduce to the test setup. The capacitance of the ggNMOS and gcPMOS ESD protection devices used in this study was measured by Firestone in [42]. A plot of the capacitance measurement is shown in figure 4.16.

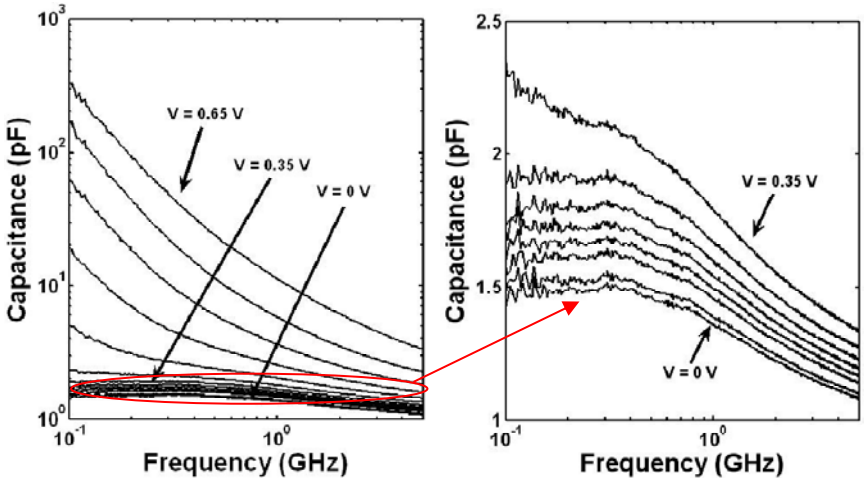

Figure 4.16: Measured small signal capacitance of the ESD protection circuits vs frequency for various input DC bias [42].

The plot shows that at zero bias the capacitance is on the order of approximately 1 pF, which is similar to the ESD protection device. Therefore it is reasonable to assume that the probe itself does not introduce any impedance that will significantly affect the accuracy of the measurement.

In order to measure the voltage gain at the input pin of the test chip, the signal generator was fixed at 50 mV while the frequency was swept in steps of 10 MHz from 100 MHz to 4 GHz. The appropriate amplifier was used for their respective frequency bands as with the previous DC measurement. The output amplitude was measured by the FET probe and recorded. From the results the voltage gain is easily calculate by simply taking the measured amplitude vs. the 50 mV input. The results of the measurement are presented in figures 4.17 and 4.18. Figure 4.17 is the measured voltage gain using the low frequency amplifier and 4.18 is the high frequency amplifier results.

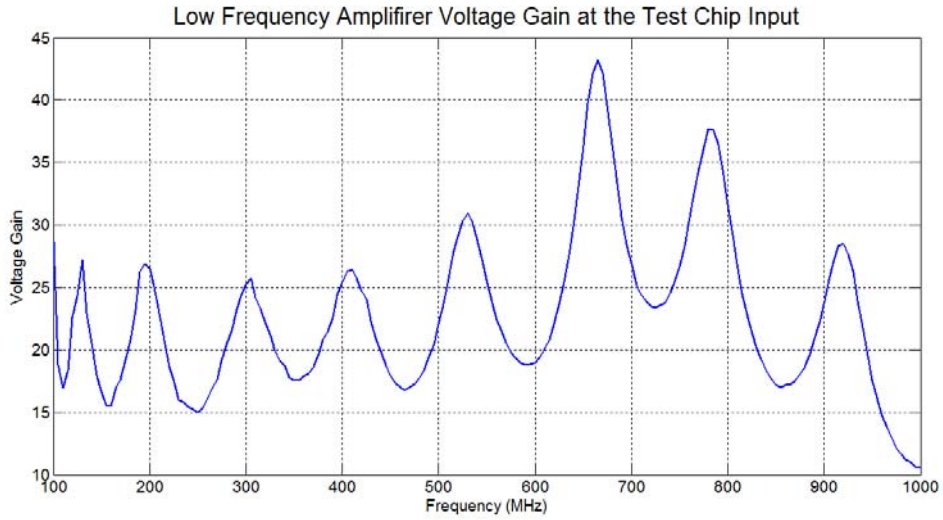

Figure 4.17: Measured voltage gain for frequencies of 100 MHz to 1 GHz

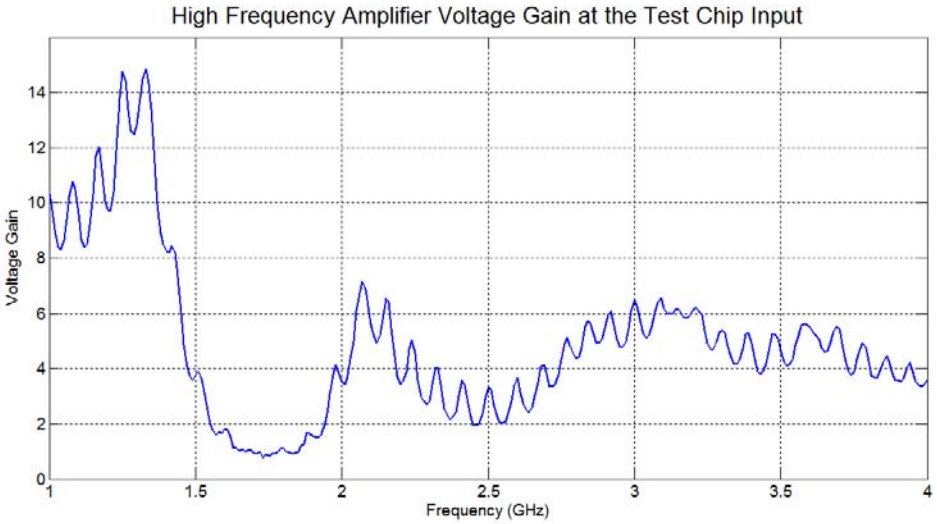

Figure 4.18: Measured voltage gain for frequencies of 1 GHz to 4 GHz

Measuring the gain in this fashion accounts for of the effects of parasitic elements and the gain variation of the amplifiers. The only exception is that once again the lead frame and ball bond wire inductance were not included. Notice that at the higher frequencies the response resembles the result shown in the DC measurement in figure 4.11. The periodic oscillation in the gain is due to the voltage amplitude vs frequency discussed in the above transmission line theory.

Using the gain measurements and knowing the signal generator amplitudes from the input DC measurements, the response of the ESD protection devices can be evaluated according to the actual voltage at the device. Figure 4.19 is a plot of the detected voltage vs. the input voltage amplitude for several different frequencies.

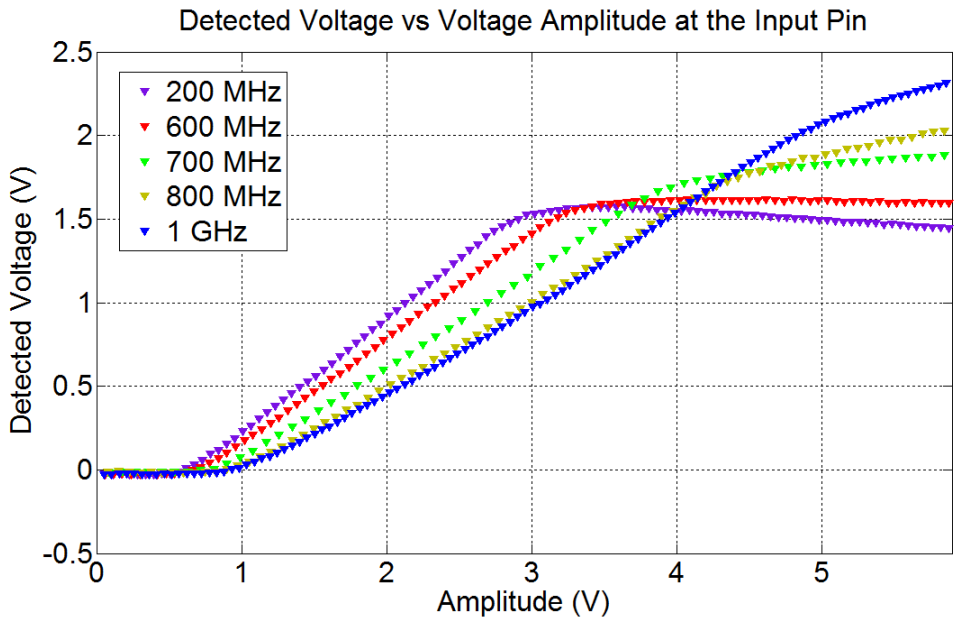

Figure 4.19: Detected voltage plotted vs. the input voltage amplitude that was calculated from the gain measurement.

The plotted frequencies were chosen to illustrate the most important threshold in the DC response of the ESD protection devices. Recall from the theory presented in 4.2

that the response should fall with increasing frequency and that the gcPMOS response should fall off faster than the response of the ggNMOS. The difference in response is due to the inherent difference in the minority carrier mobility of electrons and holes. The results plotted in figure 4.19 confirm this theoretical assessment and show good agreement with the approximation presented in figure 4.6. The plot shows a gradual decrease in the slope of the response as the frequency increases, indicating that the ggNMOS's response begins to noticeably degrade at frequencies 600 MHz and above. Above 700 MHz, the curves show that the DC response continue to rise with increasing input amplitude even once the DC voltage reaches the mid-point of 1.5 V. The inflection in the curves at the mid-point show that the gcPMOS is responding to the signal, but the response is weaker than that of the ggNMOS and the detected voltage continues to rise.

4.4 Chapter Conclusions

This chapter presented the results of experimental measurements whose purpose was to characterize the effects of HPM effects at the input stage of CMOS electronic circuits due the interaction of HPM with ESD devices. One of the most important results of this evaluation was the understanding developed of the frequency dependence of the ESD response. The result show that a significant DC offset can occur at the input of a circuit and that the severity of that offset has a great dependence on the frequency of the HPM signal. Under certain conditions the DC bias level can approach levels near the V_{dd} bias voltage.

Based on the experimental results and the theoretical treatment it can be concluded that the observed frequency dependence is due entirely to the reverse

recovery transient response of the PN junction of the devices. The reverse recovery time can be calculated to a good approximation using analytical solutions to the minority carrier diffusion equation, reverse recovery time can be used to perform a reasonable accurate calculation of the frequency dependence of the response of a PN junction-based ESD protection device. The analysis also revealed that due to the difference in electron and hole mobility, the detected voltage response of the gcPMOS begins to roll off at lower frequencies than the ggNMOS. This disparity in response is source of the input DC bias levels that exceeded the balance level of approximately 1.5 V in the experimental measurement.

The evaluation of the parasitic elements' contribution to the overall input response confirms the importance of accurately accounting for all the external linear elements present in the system. In this study measurement techniques were used to measure the effects of the parasitic elements and allowed for a true evaluation of the HPM effects based on the terminal voltage. The S-parameter measurement will also be a vital part in the accurate modeling of HPM effects presented in chapter 6.

Chapter 5 : HPM Effects in CMOS Test Circuits

5.1 Introduction

This chapter presents the results of experimental measurements performed on the CMOS digital test circuits described in Chapter 2. Measurements were performed to evaluate the voltage and current characteristics of a CMOS circuit when stressed by HPM. The output voltage waveforms and average supply current drawn by the MOS circuitry was measured and characterized in terms of the HPM amplitude and frequency driving the input. Analysis is performed to characterize the observed HPM effects and to relate these effects to the input response discussed in the previous chapter.

The purpose of the experiments and subsequent analysis is to identify the conditions whereby HMP injection causes effects such as state changes or abnormal current behavior, which could potentially generate upset events in larger systems. The first section of the chapter presents the results of experimental measurements performed on the single inverter test circuit. The results of these measurements are analyzed in the second section by comparing the behavior of the inverter under HPM excitation to the behavior predicted by established CMOS theory. The third section presents the results of experimental measurements performed on the remaining three test circuits, which were designed to represent a typical commercial device. Each observed effect is classified by the voltage and current behavior, and by the HPM drive frequency and amplitude. The fourth section of chapter is a summary and discussion of the experimental and analytical results.

5.2 Experimental Results for the Single Inverter Test Circuit

The purpose of the following experimental measurements was to study how HPM signals influence the voltage and current characteristics of the fundamental building block of CMOS circuits. The input frequency was varied from 100 MHz to 4 GHz as described in chapter 3. The RF output from the signal generator was pulsed modulated with a pulse width of 7μs and a period of 100 μs. The length of the period was chosen in order to eliminate thermal effects from influencing the measured quantities. The input power ranged from -20 dBm to 20 dBm for each frequency. For each variation of the amplitude, the following quantities were recorded:

1. The input waveform as seen through the bias circuit (see chapter 3 for bias circuit)
2. The average current measured from V_{dd} to ground during the pulse modulated HPM excitation.
3. The output voltage waveform.

Both test circuits were fully packaged and mounted onto the printed circuit boards discussed fully in chapter 3. Figure 5.1 shows the schematics for the device under test.

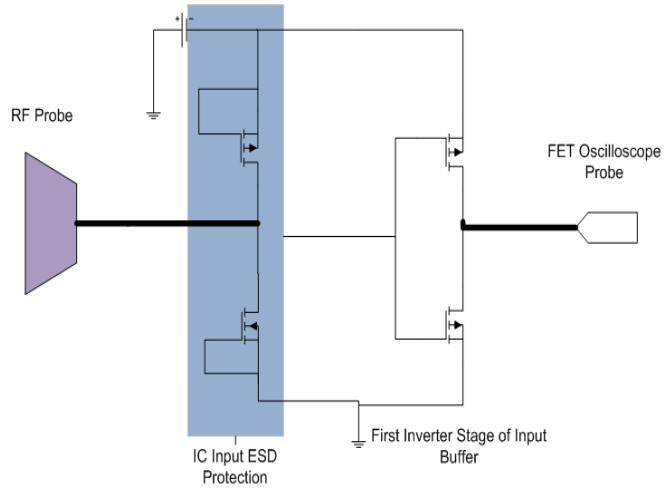

Figure 5.1: Schematics for the single inverter test circuit

5.2.1 Output Voltage Measurements

To present an overview of the measured output response of the inverter test circuit, the time averaged mean output voltage during HPM excitation was plotted for each drive amplitude and frequency. The plots, which are presented in figures 5.2 and 5.3, are created in same manner as the figures 4.9 and 4.10.

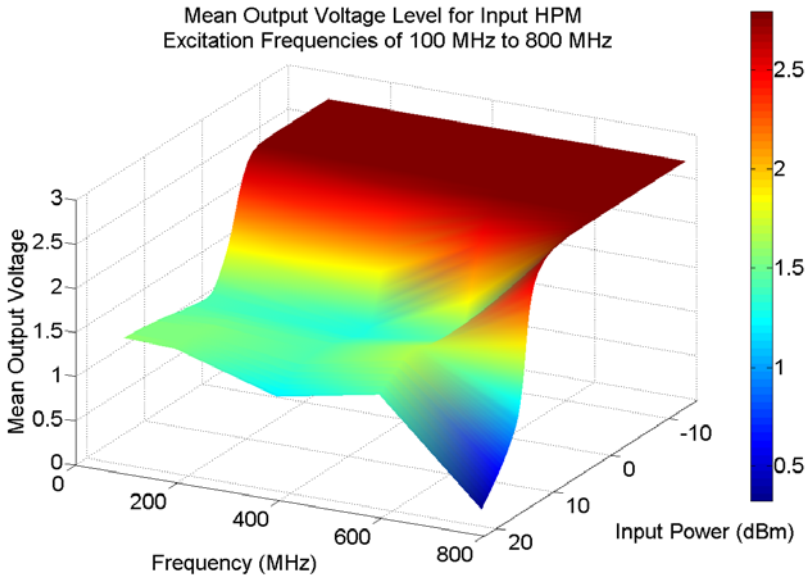

Figure 5.2: Mean output voltage vs. input RF power and frequency of the single inverter test circuit for frequencies from 100 MHz to 800 MHz.

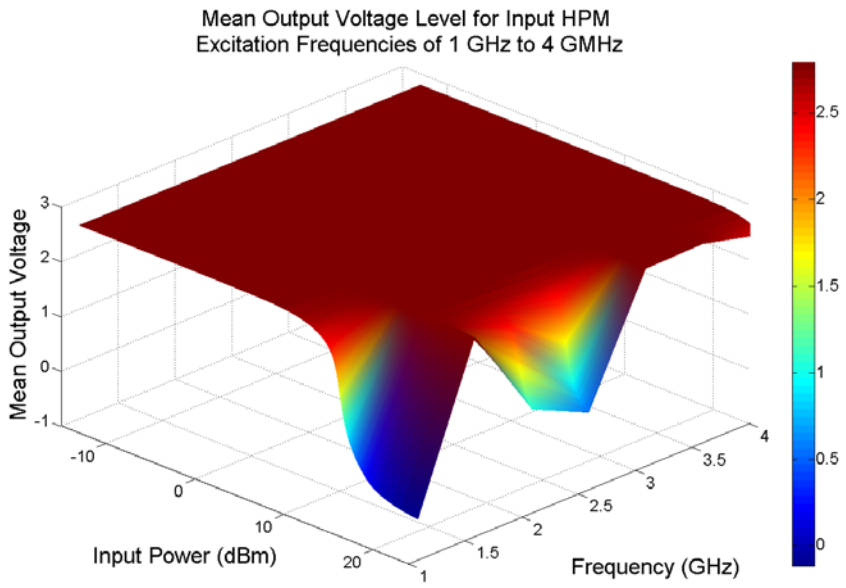

Figure 5.3: Mean output voltage vs. input RF power and frequency of the single inverter test circuit for frequencies from 1 GHz to 4 GHz.

The overall mean output voltage response corresponds to the input detected voltage measurements presented in figures 4.9 and 4.10. For frequencies of 1.5 GHz, 3.0 GHz, 3.5 GHz, and 4 GHz the output response is minimal. At these frequencies, the input detected voltage never exceeded the noise margins due to the effects of the input parasitic impedances, as shown in figure 4.10. Notice at frequencies of 800MHz, 1 GHz, and 2.5 GHz that the plot shows the mean voltage drops below $V_{dd}/2$ as the input power increases. Relating this plot to the input detected voltage measurements of the same frequencies shows that this behavior corresponds to the input detected voltage exceeding $V_{dd}/2$. For frequencies from 100 MHz to 600MHz, the plot indicates that the mean voltage plateaus at $V_{dd}/2$, which is also consistent with the response at the input shown in figure 4.9. Aside from the influences of the input parasitic elements, there is a clear shift in the output voltage behavior at 600 MHz. To illustrate this better consider the plots in figure 5.4.

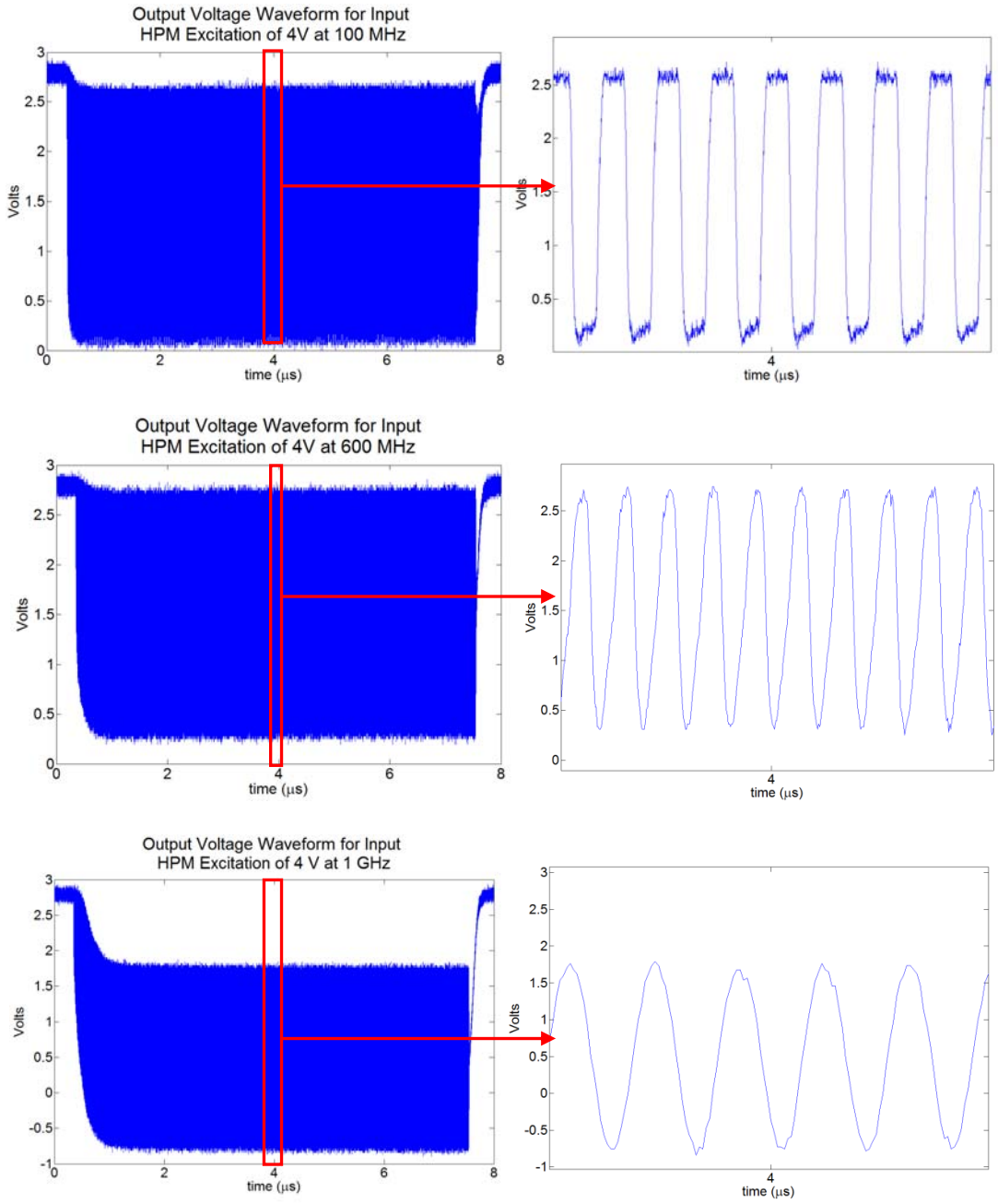

Figure 5.4: Output voltage waveforms for input HPM amplitude of 4V and for frequencies of 100 MHz (top), 600 MHz (middle) and 1 GHz (bottom). The plots demonstrate the change in the output voltage response from 100 MHz to 1 GHz

The plots in figure 5.4 are output voltage waveforms for frequencies 100 MHz, 600 MHz, and 1 GHz with the same input amplitude of 4 V as measured by the output probe described in chapter 3. The output voltage waveform for input frequency of 100 MHz resembles a logic waveform. In the previous chapter it was shown that frequencies below 600 MHz were generally in the quasi-static regime for both the ggNMOS and the ggPMOS. Under these conditions the input sinusoid is rectified by the ggNMOS, and by the ggPMOS once the input amplitude exceeds V_{dd}. The results from the output measurements show that the inverter is capable of responding in kind, and that the output waveform follows the input signal. The plot for frequencies 600 MHz and 1 GHz demonstrate how the output response changes as the frequency increases. The voltage no longer resembles a logic waveform and the peak to peak voltage decreases with frequency. At 1 GHz, the output resembles the input sinusoidal signal superimposed on a DC component. This trend continues as the frequency increases further. Consider the output voltage response at 2.5 GHz shown in figure 5.5.

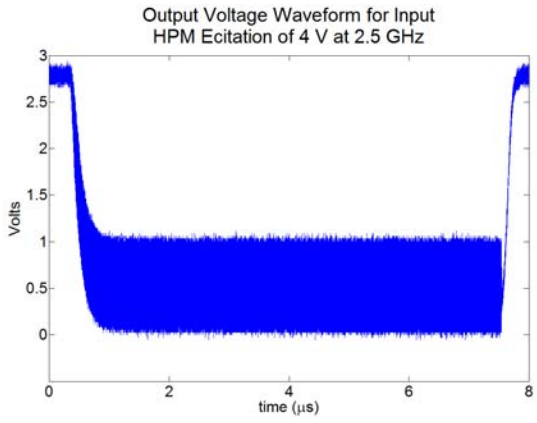

Figure 5.5: Output voltage waveform for input HPM amplitude of 4V and for frequency 2.5 GHz. The plot shows the output response resembles a single state change in the inverter that occurs for the duration of the HPM pulse.

The overall response of the output in figure 5.5 resembles a single state change at the inverter output that lasts for the duration of the HPM excitation.

Overall, the results of the output measurements demonstrate two key behaviors. For frequencies below 600 MHz, the output of the inverter follows the input signal, and state changes occur at the same frequency as the input drive frequency. For frequencies above 600 MHz, the voltage amplitude at the output diminishes with increasing frequency and the device no longer changes state at the frequency of the input signal. However, the DC level of the output shifts in correspondence with the detected voltage at the input, which results in a single state change for the duration of HPM interference.

5.2.2 Current Measurement Results

The results of the current measurements are plotted in figures 5.6 and 5.7. The plots show the average current measured during the HPM pulse vs the input power and frequency.

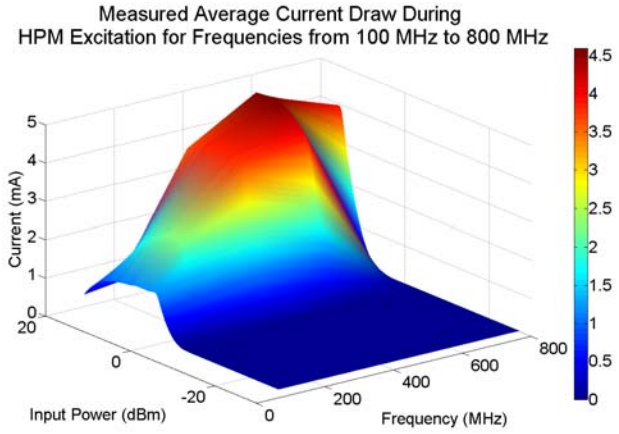

Figure 5.6: Average current vs. input RF power and frequency of the single inverter test circuit for frequencies from 100 MHz to 800 MHz.

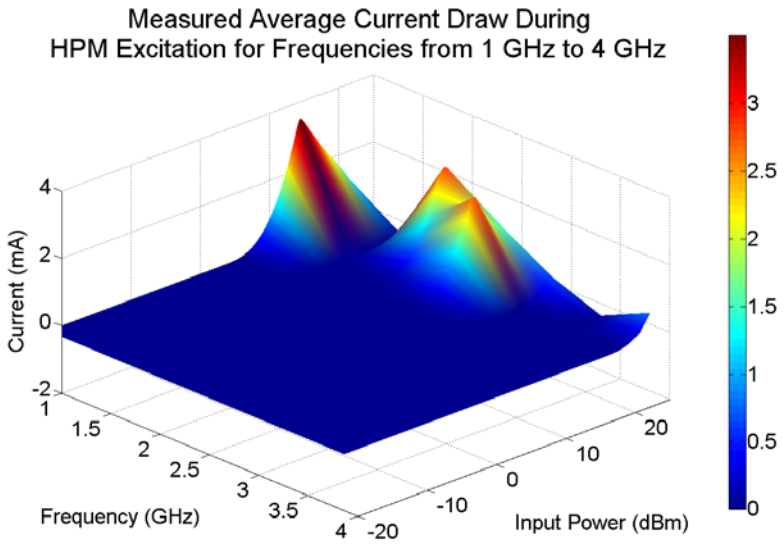

Figure 5.7: Average current vs. input RF power and frequency of the single inverter test circuit for frequencies from 1 GHz to 4 GHz.

As expected, there is little current draw for frequencies of 1.5 GHz, 3.0 GHz, 3.5 GHz, and 4 GHz where the input response is minimal due to the parasitic impedances. There are two intriguing characteristics to the behavior of the average current as presented in figures 5.6 and 5.7. First, notice that the maximum average current initially increases with frequency up to 600 MHz, but then decreases with frequency beyond 600 MHz. Secondly, for frequencies up to 600 MHz, the average current increases with input power and plateaus at approximately 1 to 3 dBm. However, for frequencies above 600 MHz the current increases with input power until it peaks and then begins to decline. To examine these characteristics further, consider the plots presented in figures 5.8 and 5.9. Figure 5.8 is a plot of the average current measured for frequencies of 100 MHz, 200 MHz, 400 MHz, and 600 MHz vs. the input voltage amplitude. The amplitude of the input is determined in the same manner discussed in detail in the previous chapter.

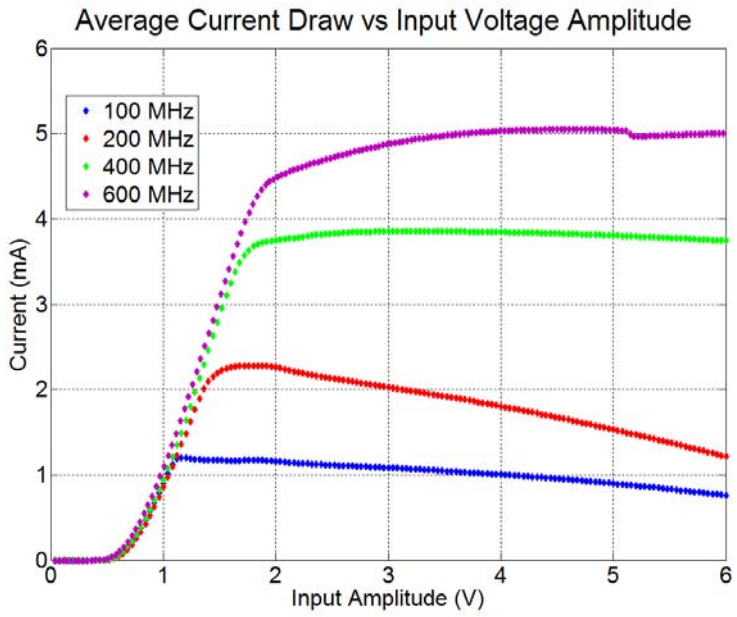

Figure 5.8: Average current draw vs. input voltage amplitude for frequencies from 100 MHz to 600 MHz for the single inverter test circuit.

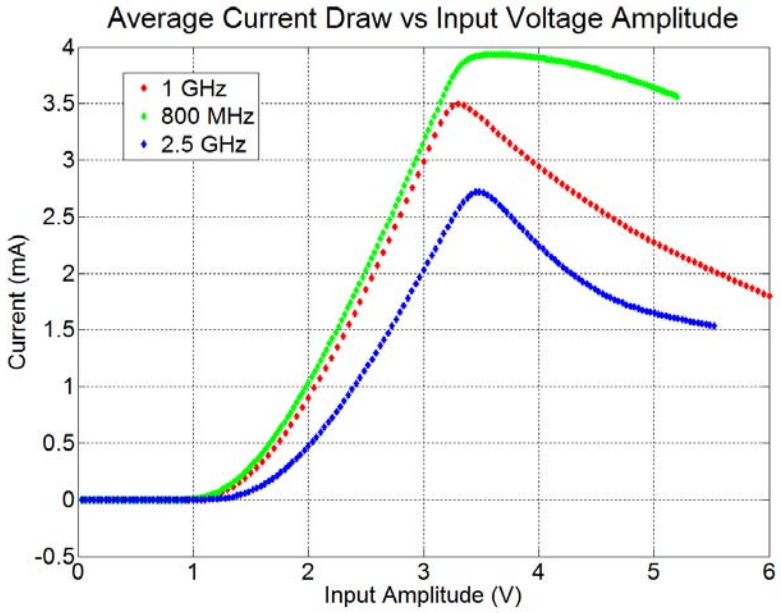

Figure 5.9: Average current draw vs. input voltage amplitude for frequencies from 1 GHz to 4 GHz for the single inverter test circuit.

After the current plateaus in figure 5.8, there is a decline in the average current as the input amplitude increases. This is likely due to RF current feeding through the ggPMOS as the input amplitude exceeds V_{dd}. Although the local bypass capacitor is a very good high frequency capacitor, there is some equivalent series resistance (ESR) associated with the deivce that will prevent it from being a perfect RF short to ground. Inevitably, some portion of the RF current will feed back through the picoameter and superimpose with the current being drawn from the power supply. The peak current value for frequencies 100 MHz to 400 MHz increase approximately linearly while the current measured for 600 MHz deviates from this trend. This suggests a transition in circuit response at 600 MHz similar to what is observed in the voltage measurments.

Figure 5.9 is a similar plot to 5.8 for frequencies of 800 MHz, 1 GHz, and 2.5 GHz. This plots demonstrates the clear change in current behavior at frequencies above 600 MHz. The curves resemble a DC transfer curve of an inverter in that they rise to a peak value analogous to the behavior of an inverter when the DC bias is $V_{dd}/2$. The peak current decreases with input drive frquency in a similar manner that the peak to peak voltage decreases at the same frequencies, which suggests a possible corrolation.

5.3 Analysis of Experimental Measurements on the Single Inverter Test Circuit

The following section presents the analysis of the experimental results for the single inverter test circuit. The analysis utilizes established theory found in literature for MOSFET transistor switching characteristic and transient CMOS current behavior.

5.3.1 Analysis of Output Voltage Measurements

For frequencies below 600 MHz, the experimental results show that the output voltage follows the input voltage, and as the HPM amplitude increases beyond V_{dd} the output voltage resembles a logic waveform. For frequencies above 600 MHz the behavior changes and the output voltage amplitude no longer follows the input. The following analytical treatment is used to explain the change in behavior of the output voltage by examining the switching speed of a MOSFET device. The hypothesis is that as the frequency increases, the voltage at the input switches faster than the output can charge the load capacitance. As the frequency increase more, the load capacitance will charge less as the voltage at the input switches more rapidly, which would explain why the voltage amplitude at the output diminished at frequencies above 600 MHz. The equivalent circuit use for this analysis is shown in figure 5.10.

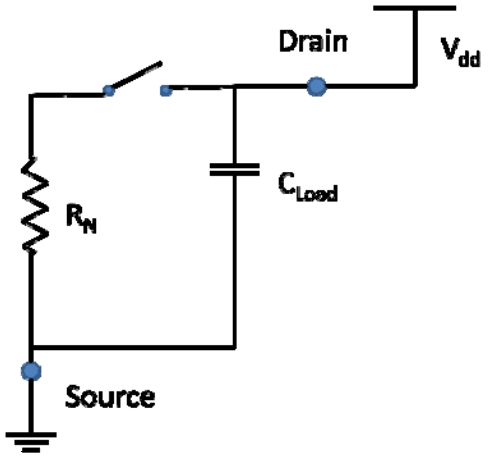

Figure 5.10: Simple digital MOSFET model used to approximate the maximum the switching speed of the single inverter test circuit.

For this analysis it is assumed that, once the switch is closed, the channel is formed and the device is in saturation. The charging of the load capacitance is governed by the time constant $\tau = R_N C_{Load}$. R_N is the resistance between the drain and the source

when the device is in saturation. This resistance is often referred to as the switching resistance and is given in equation (2.1). The equation for the time constant is thus given by equation (5.1) where k is defined in equation (2.2) [44].

$$\tau = \frac{2L \cdot V_{dd}}{k_{n,p} W \cdot (V_{dd} - V_{th})^2} \cdot C_{Load} \tag{5.1}$$

This approach is very similar to the analysis use to approximate the process characteristic time constant. The difference is the capacitance used to calculate the process time constant is the intrinsic MOSFET capacitances.

The time constant in (5.1) will be used to approximate the rise time of the voltage across the output load capacitance once the switch is closed. The time for the voltage to transition from 10% of its initial value to 90 % of its final value is 2.2τ. The following three elements contribute to the total load capacitance of the test circuit: the capacitance of the output probe, the parasitic capacitance of the ball bond wires and packaging, and the parasitic capacitance of the board trace. The approximate capacitance of each element is presented in table 5.1.

Table 5.1: Approximate values for each element of the total load capacitance of single inverter test circuit

Element	*Capacitance*
Probe	1 pF
Packaging	0.7 pF
Board trace	1.2 pF

The capacitance of the package elements was obtained from measurements of a similar LCC 44 package found in [57]. The board trace capacitance was calculated

using the physical dimensions of the trace and the permittivity of the board material. The total load capacitance is therefore estimated to be approximately 3.0 pF. Using the dimensional parameters for the PMOS of the inverter from table 2.4 and the device parameters extracted from the process test wafer (see Appendix A) the effective switching resistance is calculated to be 246.6 Ω. Using the calculated resistance value and the estimated load capacitance, (5.1) yields a time constant of 0.74 ns and an output voltage rise time of 1.63 ns. Based on the calculated rise time, the estimated maximum switching frequency of the inverter is 615 MHz. It is important to point out a limiting factor to this approximation. The calculation above does not account for short channel effects; most notably, the effects of velocity saturation in the channel. Velocity saturation in short channel MOSFETS (channel lengths less than 1 μm) reduces the carrier motilities in the channel increasing the effective switching resistance [44]. For deep sub-micron processes, the effects of velocity saturation should be accounted for when making similar approximations.

The results of the analysis show that the change in amplitude of the output voltage is due to the limited ability of the device to drive the output load at frequencies above 600 MHz. The plot of the output voltage for 600 MHz in figure 5.4 shows that the output amplitude is slightly diminished when compared to 400 MHz for the same input amplitude. This suggests that the actual limiting frequency is slightly lower than 600 MHz. However, the result of the analysis provides a very good approximation for the frequency beyond which the output voltage behavior changes for sinusoidal HPM excitation. In chapter 2, the frequency limit for normal digital operation was estimated by measuring the propagation delay under the same

load conditions as the experimental measurements, which predicted a very similar limit frequency of 592 MHz.

5.3.2 Analysis of Current Measurements

The following section presents the analysis of the current measurements for the single inverter test circuit. Similar to the results in the voltage measurements, there is a transition in current behavior for frequencies above 600 MHZ. The following analysis examines the current behavior of the inverter under HPM excitation using common techniques found in literature, and correlates the observations in the current measurements to the behavior of the output voltage.

One of the great advantages of CMOS technology is that it draws no DC current in the static state (excluding the consideration of sub-threshold leakage currents) [44]. Current draw in CMOS only occurs when devices change state. The transient current that occurs when an inverter switches state consists of two components commonly referred to as the dynamic current and the short circuit current.

The dynamic current considers the ideal switching of the inverter, in which the PMOS or NMOS turn on or off instantaneously depending on the initial state of the inverter. When the voltage at input of the inverter transitions from low to high, the NMOS will switch off and the PMOS will switch on. Current flows through the PMOS, which charges the load capacitance of the output. When the voltage switches the other way, the capacitor will discharge through the NMOS to ground [44, 45]. Figure 5.11 shows a schematic diagram of dynamic current. C_{tot} represents the total

capacitance, which includes all the parasitic capacitance of the device as well as the actual load capacitance of the next stage of the circuit.

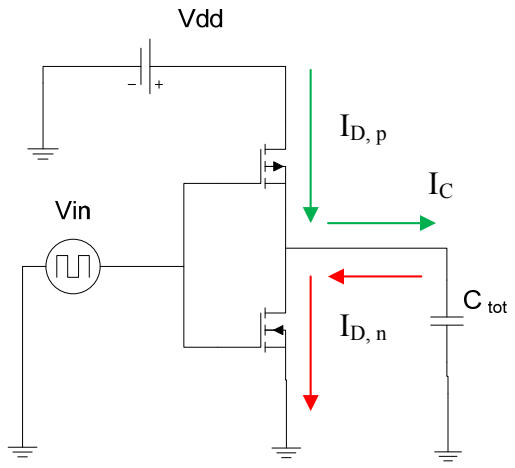

Figure 5.11: Schematic diagram of dynamic current in a CMOS inverter

The dynamic current for periodic excitation is a linear function of frequency given by equation (5.2) [45].

$$I_{avg} = C_{tot} V_{dd} f \tag{5.2}$$

Notice that the dynamic current is only dependant on the output capacitance and frequency, and does not depend on any other device parameters, which means that equation (5.4) will apply CMOS devices in general [44, 45].

The second component of the transient current is often referred to as the short circuit current. Real logic waveforms do not have instantaneous rise times. For a period of time during the rise or fall of the input signal when the voltage resides above the NMOS threshold voltage and below the PMOS threshold voltage (with respect the rail voltage), both the NMOS and PMOS will conduct creating a path to ground through the inverter. This process is illustrated in figure 5.12.

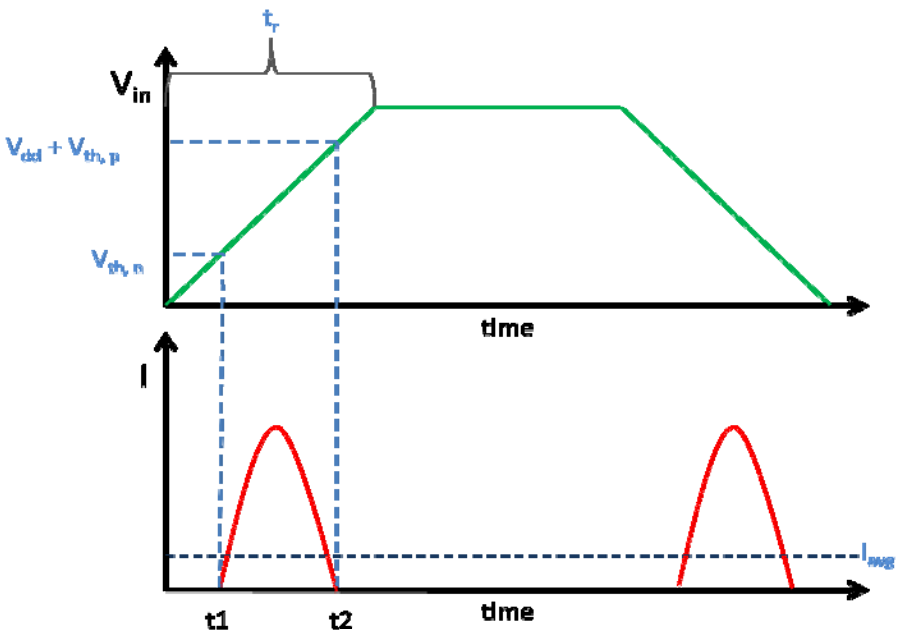

Figure 5.12: Short circuit current in a CMOS inverter during full state changes.

The average short circuit power for a square pulse input signal is given by equation 5.3 [59].

$$P = I_{avg} \bullet V_{dd} \tag{5.3}$$

Calculating the average short circuit current is simplified by making the following assumptions:

1. The transistors are balanced
2. The rise time and fall time are equal

Assumption 1 requires that $\beta_p = \beta_n$ where,

$$\beta = \mu_{n,p} C_{ox} \frac{W}{L} \tag{5.4}$$

$\mu_{n,p}$ is the surface mobility of electrons and holes respectively and C_{ox} is the gate capacitance per unit area [52]. Assumption number 2 means that only current from *t1* to $t_r/2$ needs to be evaluated due to symmetry. From time *t1* to *tr/2* the NMOS

transistor will be in saturation and the current through the inverter will be given by equation (5.5) [52].

$$I = \frac{\beta}{2}\left(V_{in} - V_{Th,n}\right)^2 \tag{5.5}$$

Therefore, the average short circuit current can be determined by evaluating the integral in equation 5.6 [59].

$$\mathrm{I}_{avg} = \frac{4}{T}\int_{t1}^{tr/2} \frac{\beta}{2}\left(V_{in}(t) - V_{Th,n}\right)^2 dt \tag{5.6}$$

Evaluating equation 5.6 yields the expression given in equation (5.7) [59].

$$I_{avg} = \frac{\beta}{12 \cdot V_{dd}}\left(V_{dd} - 2V_{th,n}\right)^3 t_r f \tag{5.7}$$

The most important difference between the dynamic current and the short circuit current is that the short circuit current is also linearly proportional to the transistor dimensions.

The above analytical expressions are used to calculate the average current of the test circuit to compare with the measured current response. Each analytical equation assumes that the input voltage amplitude is sufficiently high to fully switch the state of the CMOS device. In figure 5.8, the current plateaus when the input amplitude of the RF is high enough to switch the output state of the test circuit. Therefore the calculated value will be compared to the maximum average current measured. Figure 5.13 demonstrates the accuracy of the calculation at low frequency and the relative contribution of each of the current components.

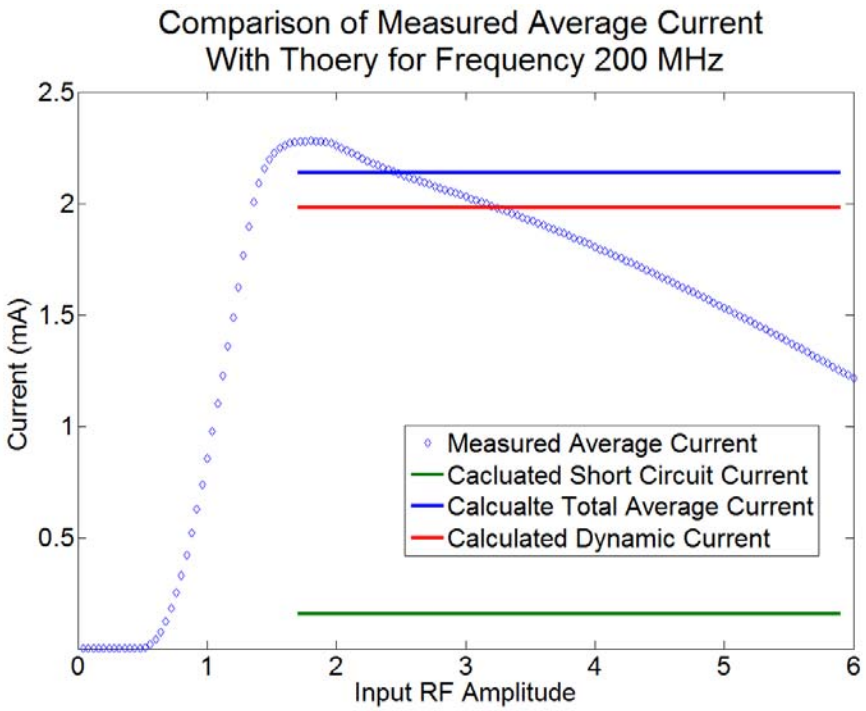

Figure 5.13: Measured average current for input drive frequency of 200 MHz compared to theoretical calculation of the average current for full transistor switching.

The capacitance value used for C_{tot} is the same estimated output capacitance of 3 pF used in the previous section. It is assumed that the output load capacitance is much larger than any of the intrinsic device capacitances. Since the input of the test circuit is sinusoidal the ratio of the rise time to the period is kept at a constant value of ¼ of the period in equation (5.7).

Figure 5.14 is a plot of the theoretical calculation of the average current versus frequency compared to the maximum measured average current at each of the experimental frequencies. The theory accurately predicts the maximum average current for frequencies of 100 MHz to 400 MHz. At 600 MHz the maximum average current deviates from the calculated value, which corresponds to the maximum switching frequency presented in the previous section.

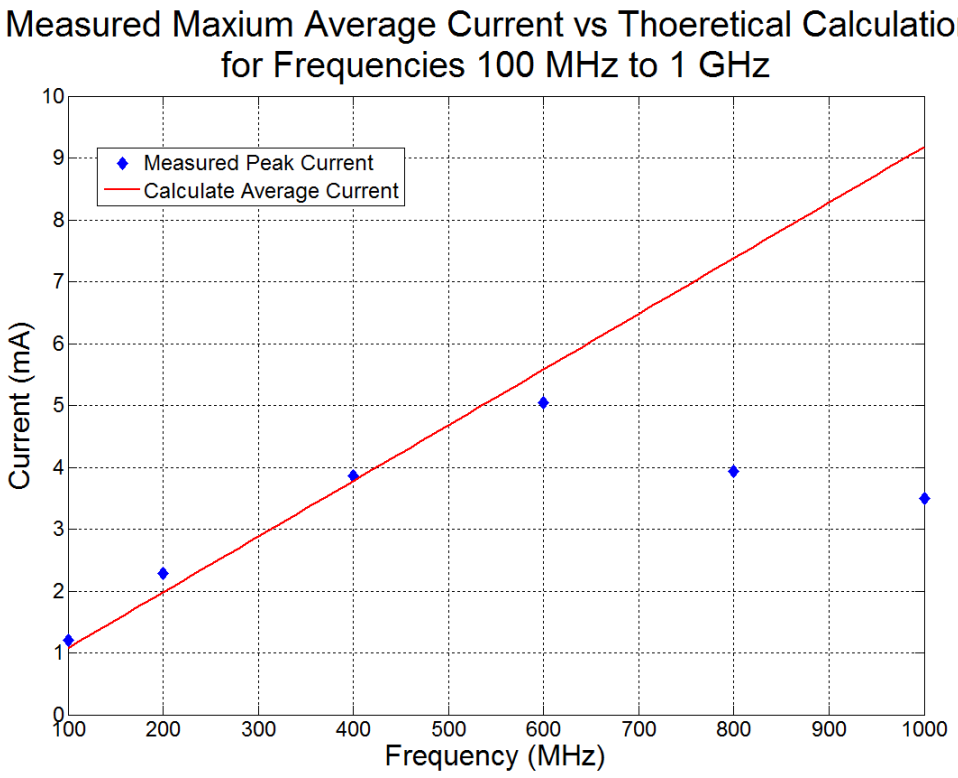

Figure 5.14: Measured maximum average current values compared to theoretical calculation for the single inverter test circuit.

In order to analyze the current behavior for frequencies beyond 600 MHz, consider the plots in figures 5.15 and 5.16. The plots show the measured input detected voltage, mean output voltage, and average current versus input amplitude for drive frequencies of 1 GHz and 2.5 GHz. Comparing the current curve to the voltage curves, the peak of the current occurs at the center of the output voltage transition when the input detected is approximately 1.5 V. This behavior is very similar to a DC current transfer curve. The output voltage measurements show that the output voltage amplitude is small compared to the DC component. Therefore, the device is biased into conduction as the input amplitude increase. In this situation, the short circuit current will contribute more to the total average current.

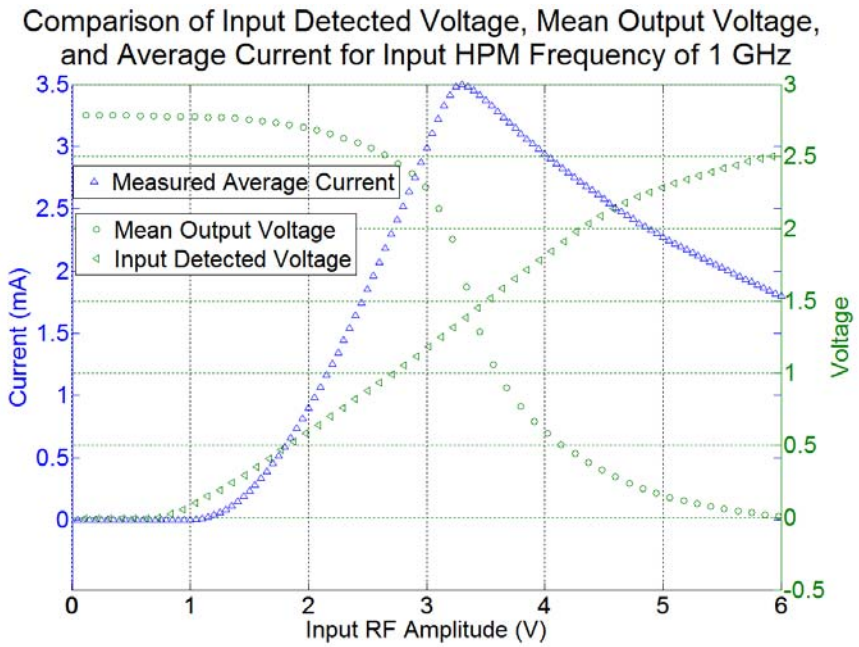

Figure 5.15: Comparison of the measured average current to the input detected voltage and the mean output voltage of the single inverter test circuit, with input drive frequency of 1 GHz.

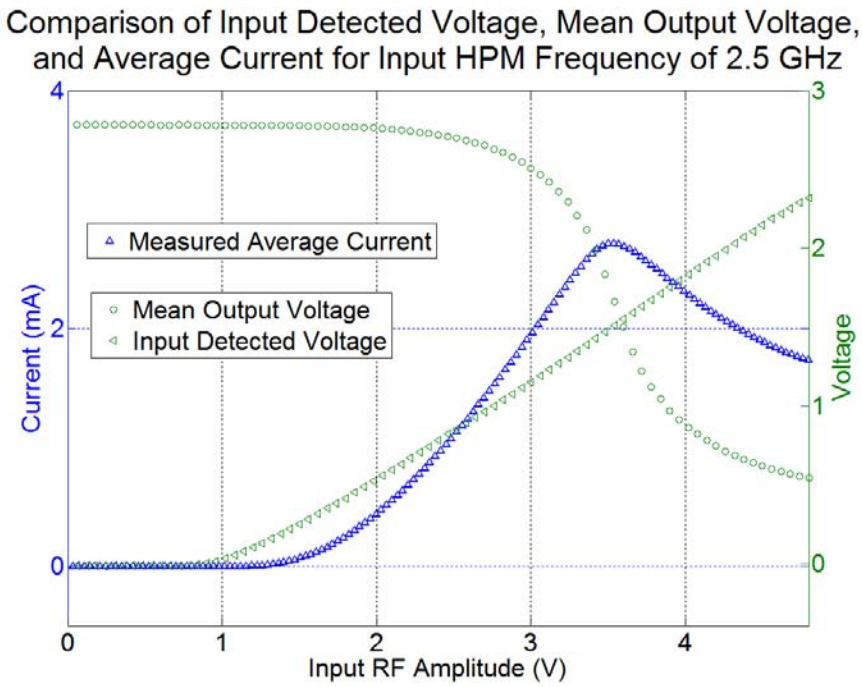

Figure 5.16 : Comparison of the measured average current to the input detected voltage and the mean output voltage of the single inverter test circuit, with input drive frequency of 2.5 GHz.

In contrast, at lower frequencies where the device switches fully the dynamic current, caused by the charging and discharging of the load capacitance, is the largest portion of the total average current as shown in figure 5.13.

At frequencies above 600 MHz, dynamic current still contributes to the total average current. The conductivity of the channel of the PMOS changes relative to the NMOS channel to cause the voltage oscillations measured across the output capacitance. The decrease in the peak current with increasing frequency is due to the diminishing amplitude of the output voltage. Essentially, the total charge on the output capacitance changes less with increased frequency, and this must be due to dynamic component since it alone accounts for charging and discharging of the output capacitance. The relative value of the dynamic component can be inferred by comparing the DC transfer curve in figure 5.17 to the current curves in figures 5.15 and 5.16. As the frequency increases, the total average peak current approaches the peak current from figure 5.17.

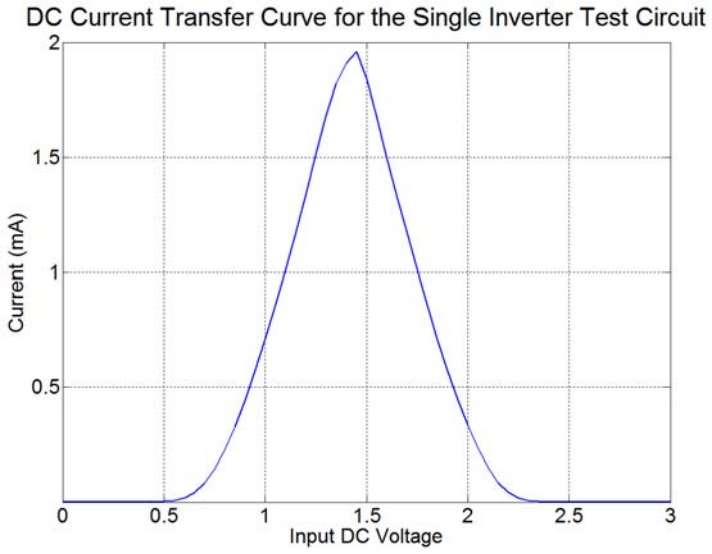

Figure 5.17: DC transfer curve for the single inverter test circuit.

5.3.3 Summary of Analysis

The experimental results and subsequent analysis for the single inverter test circuit have shown that the change in the circuit's voltage and current response to HPM signals above 600 MHz is directly related to the maximum switching speed of the device. The switching speed was determined by calculating the rise time of the output voltage using the effective switching resistance of the device and the load capacitance. Estimating the maximum switching frequency using the measured propagation delay, which is related to the switching speed of the device, provided a similar result as the estimation based on the rise time. HPM effects below this threshold frequency will be referred to as *in-band* effects, while effects above it will be referred to as *out-of-band* effects. At in-band HPM frequencies, the single inverter circuit responds in manner similar to a normal digital excitation as the HPM amplitude increases above the noise margins, and the current behavior is predicted from established CMOS circuit theory. At out-of-band HPM frequencies, The DC component at the input generated by the input ESD protection circuits dominates the circuit response. The short circuit current increases due to the input DC bias, which causes the device to conduct current as the input amplitude increases. In contrast, the dynamic current is diminished due to reduced voltage amplitude at the output.

5.4 Experimental Measurements of CMOS Digital Test Circuits

The following section presents the results of the experimental measurements of HPM effects on the fully package CMOS digital test circuits. The test circuits are the inverter chain, the JK flip-flop, and the 4 bit counter described in Chapter 2. Each of the CMOS digital test circuits were subjected to the same measurement frequencies

and input power as the single inverter circuit in the previous section. The maximum speed of each circuit is estimated from the delay measurements presented in chapter 2, and this frequency is used as the dividing point between in-band and out-of-band effects.

5.4.1 In-Band HPM Effects

The estimate of maximum switching frequency for the inverter chain circuit is 340 MHz. For the JK flip-flop and 4 bit counter limit is approximately 140 MHz. This section presents an overview of the voltage and current effects observed below these characteristic frequencies. Figure 5.18 is the measured mean output voltage for each of the test circuits for in-band HPM excitation.

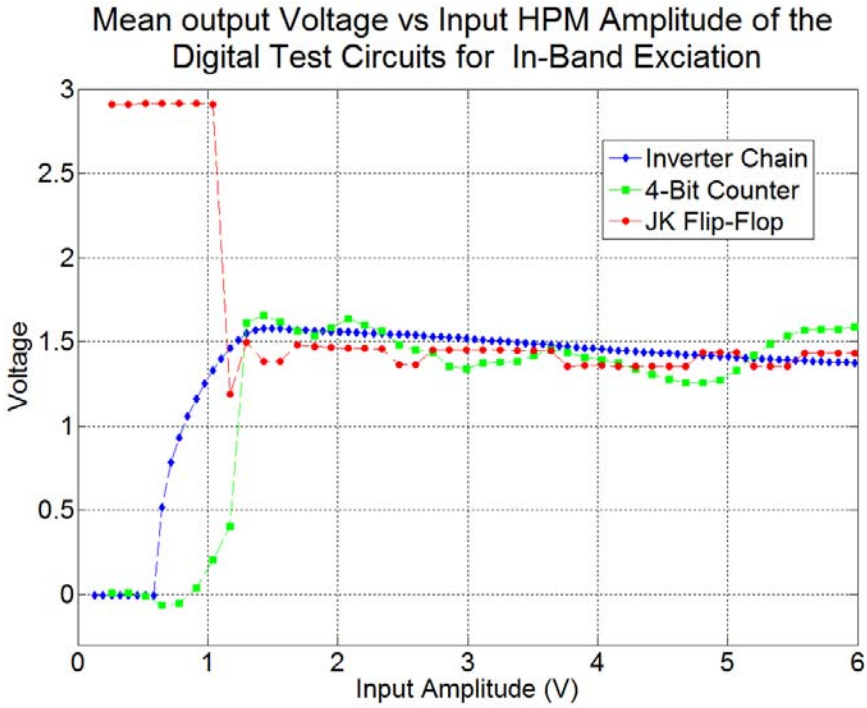

Figure 5.18: Mean output voltage of the digital test circuits versus the input amplitude. The inverter test circuit was driven at 200 MHz. The JK flip-flop and 4-bit counter were driven at 100 MHz.

The JK flip-flop and the 4-bit counter are both driven at a frequency of 100 MHz, and the inverter chain circuit was driven at a frequency of 200 MHz. For the 4-bit counter, the output plotted is the most significant bit. The plots show that the onset of full output oscillations occurs at input amplitude of approximately 1.2 V for each of the test circuits. The in-band response of 3 digital test circuits is similar to the response observed in the single inverter test circuit. Once the input amplitude reaches a level capable of switching the device, the output begins to oscillate in response to the input signal.

In order to examine the output voltage further, consider the plots in figure 5.19. The plots represent the output voltage waveforms of each test circuit for input amplitude of 4 V, and for the same drive frequencies as the data presented in figure 5.18. Similar to the results of the single inverter measurements, the output voltage resembles the response to a typical logic waveform at the input. Figure 5.20 is the magnitude of the output voltage spectrum for each of the test circuits for the same input drive frequency and amplitude presented in figure 5.19. The spectrum plots indicate that the output response frequency is directly related to the input frequency. For the inverter chain the output is the same as the drive frequency. The flip-flop is a negative edge trigger device and divides the frequency by 2; therefore the output frequency is 50 MHz. Similarly, the 4 bit counter divides the frequency by 2 for each successive bit from least significant to most significant. The most significant bit divides the frequency by 16, which should produce an output frequency of 6.25 MHz.

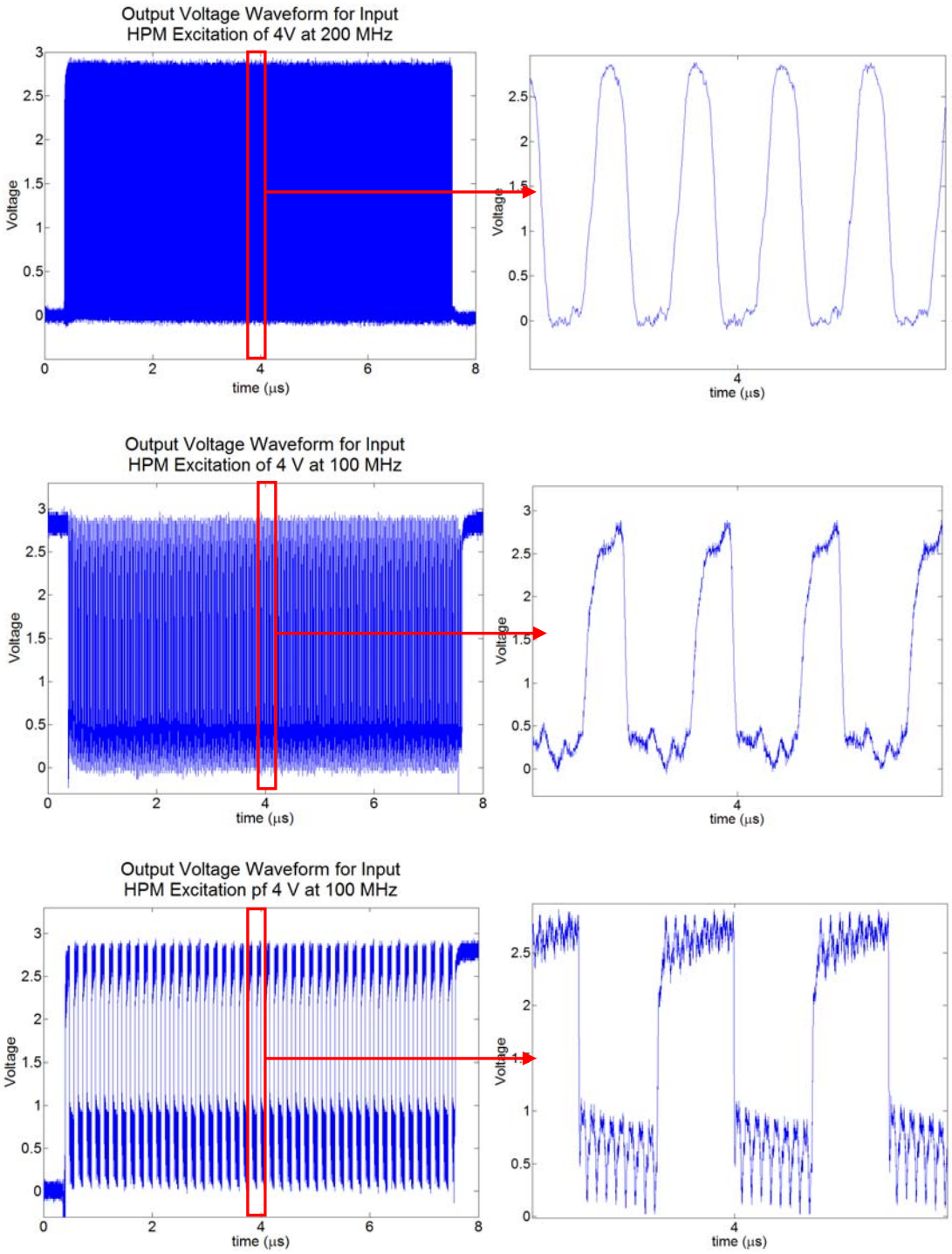

Figure 5.19: In-band output voltage response for the inverter chain circuit (top), the JK flip-flop (middle), and the 4-bit counter.

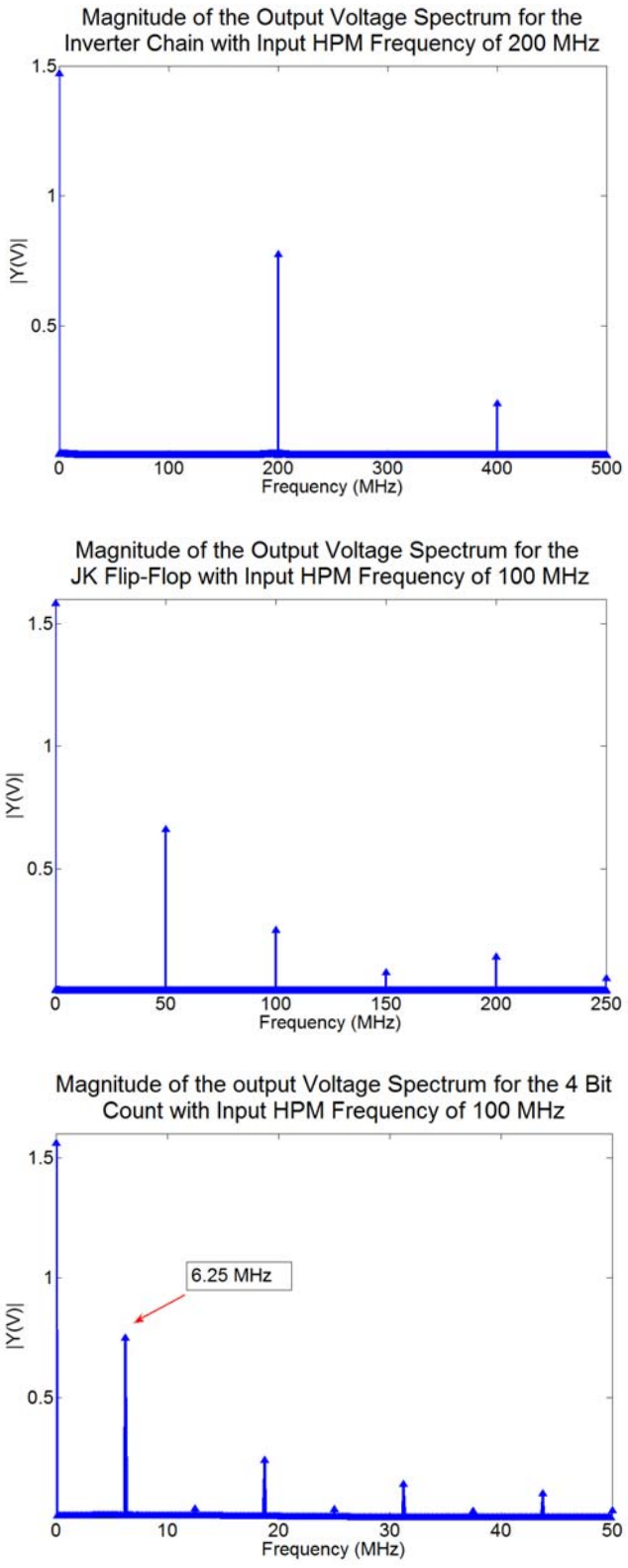

Figure 5.20: Output voltage spectrum for in-band HPM excitation for the inverter chain circuit (top), the JK flip-flop (middle), and the 4-bit counter.

The average current corresponding to the voltage measurement presented in figure 5.18 is plotted for each circuit in figures 5.21, 5.22, and 5.23. The measured average current is plotted as a function of input HPM amplitude. Additionally the red marker in each plot is the average current measured for normal digital excitation (amplitude of 3 V), which was presented in chapter 2 (see figure 2.22). Since 200 MHz was beyond the measurement capability of the current measurements presented in chapter 2, the average current for normal digital excitation of the inverter chain circuit was linearly extrapolated from the measured values.

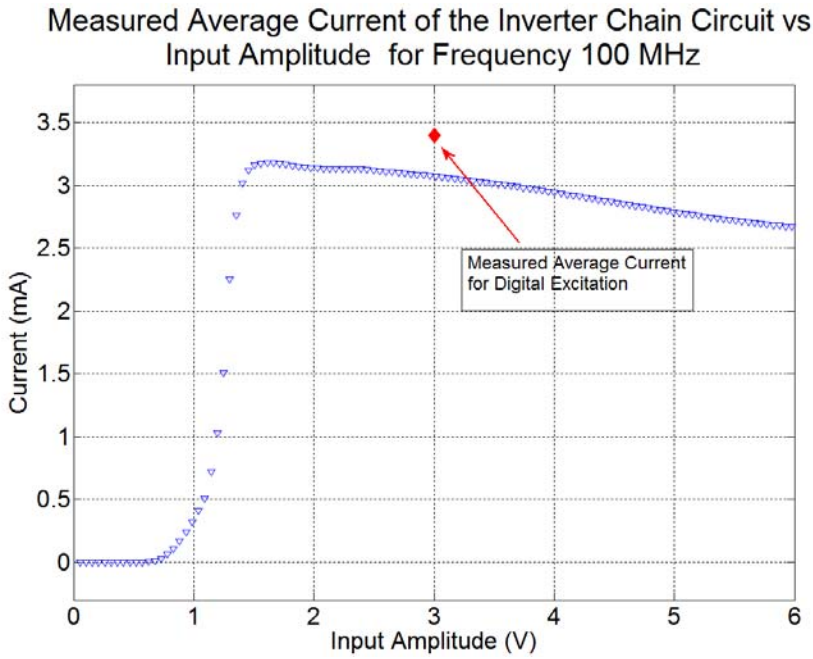

Figure 5.21: Measured HPM induced current compared to normal operation current for the inverter chain test circuit.

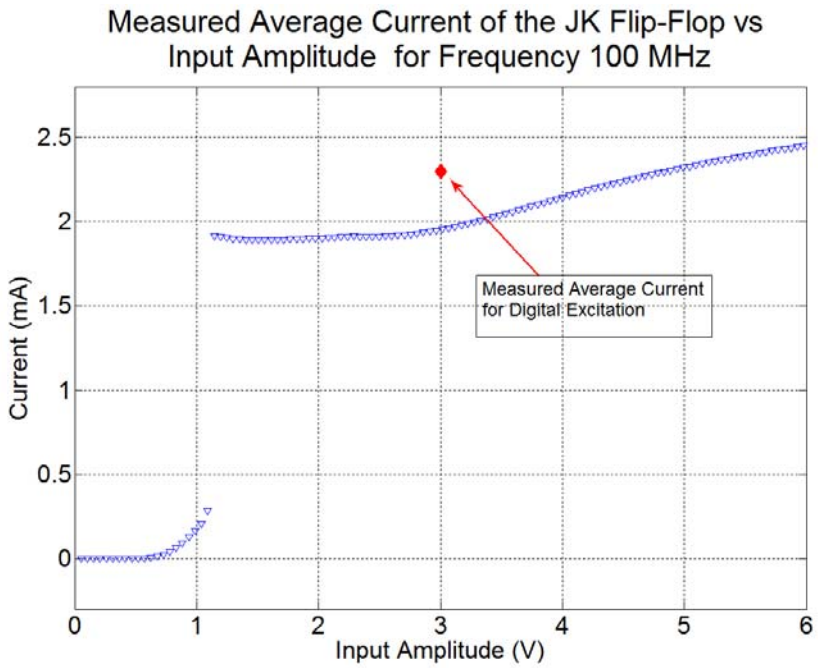

Figure 5.22: Measured HPM induced current compared to normal operation current for the JK flip-flop test circuit.

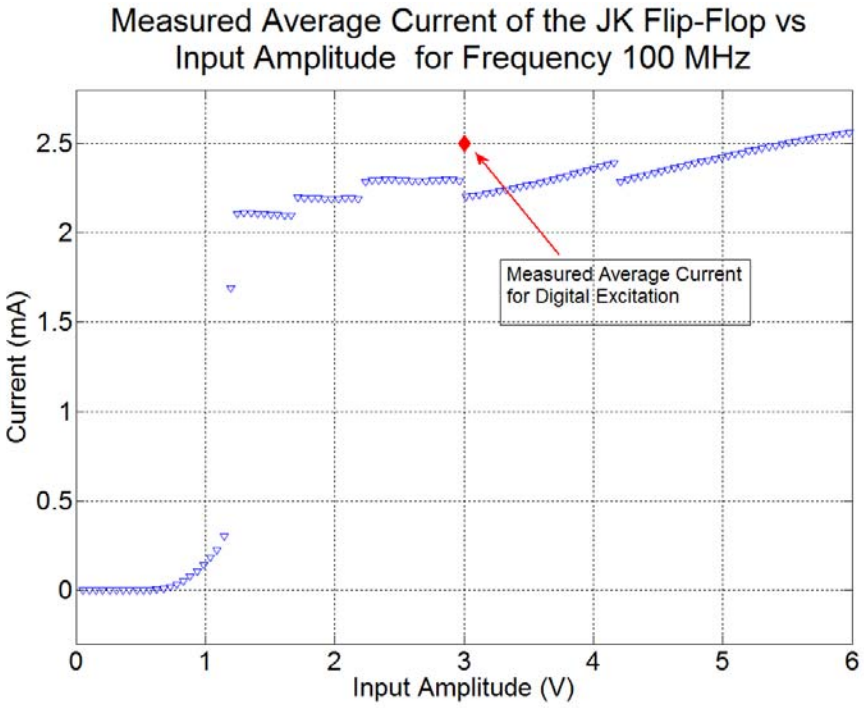

Figure 5.23: Measured HPM induced current compared to the current measured under normal digital excitation for the 4 bit counter test circuit.

Once the output begins to oscillate, the average current is relatively constant with increases HPM amplitude. Also, the peak value of the average current is comparable to the average current measured under normal digital excitation.

For in-band HPM excitation, the results confirm that the circuit response is similar to the response of a digital signal as was observed for the single inverter circuit. Bit errors occur at a rate equal to the circuits expected response to a digital signal with the same frequency as the HPM signal. Therefore, the average current will comply with expected values and increase linearly with frequency for in-band signals.

5.4.2 Out-of-Band HPM Effects

As the input frequency exceeds maximum switching speed of the circuit, some very interesting effects were observed from the experimental measurements. The observed effects can be grouped into two categories:

1. Single bit errors
2. Spurious oscillations

The above out-of-band effects were observed in all three test circuits. This section will examine the general characteristics of these two effects using experimental measurements from each of the test circuits. A complete summary of the frequency and amplitudes for which these effects occurred in each of the circuits is reserved for the next section.

For the inverter chain circuit single bit errors consist of a state change that persists for the duration of the HPM pulse. The JK flip-flop and the 4-bit counter are computational circuits that store previous states; therefore single bit errors produced by out-of-band HPM excitation are stored by these circuits after the HPM pulse. In or

to examine the properties of single bit errors consider the plot of the mean output voltage for each of the test circuits in figure 5.24. For input HPM drive frequency of 2.5 GHz all three test circuits produces single bit errors.

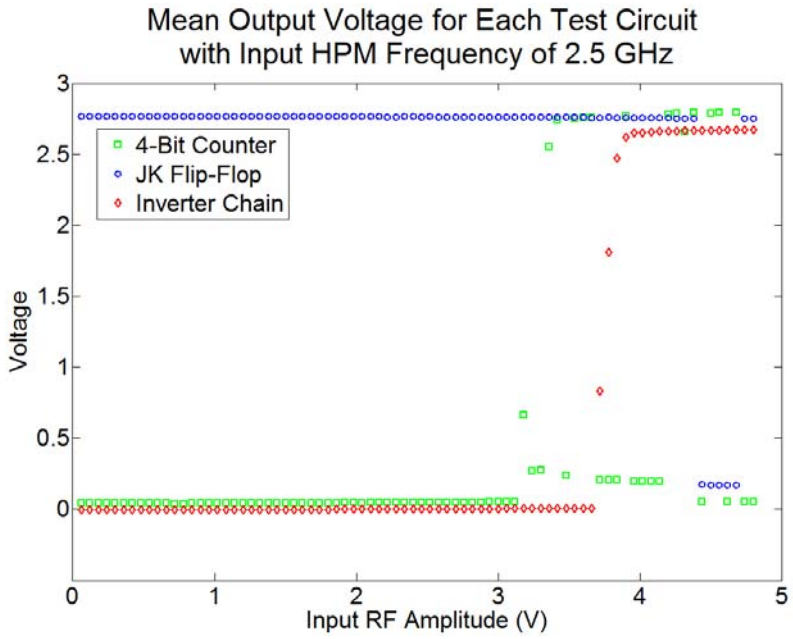

Figure 5.24: Mean output voltage of each of the digital test circuits for HPM excitation frequency of 2.5 GHz. The plot demonstrates the onset of HPM induced single bit errors.

The figure shows a sharp transition from no response to a single state change as the RF amplitude increases. Notice that the measured output voltage of the counter and flip-flop appears to oscillate between 3 V and ground. This is not an actual oscillation. During experimental measurement, the final output state of the flip will persist until the next RF pulse. When the data was recorded, either state is possible since the initial state could either be high or low. This is what creates the appearance of oscillation. The voltage and current characteristics of this effect are very similar for each of the three test circuits. Figure 5.25 is an example of a single bit error in the inverter chain circuit. The output waveform looks very similar to a waveform that

would result from a typical logic signal. The corresponding average current measurement is shown in figure 5.26.

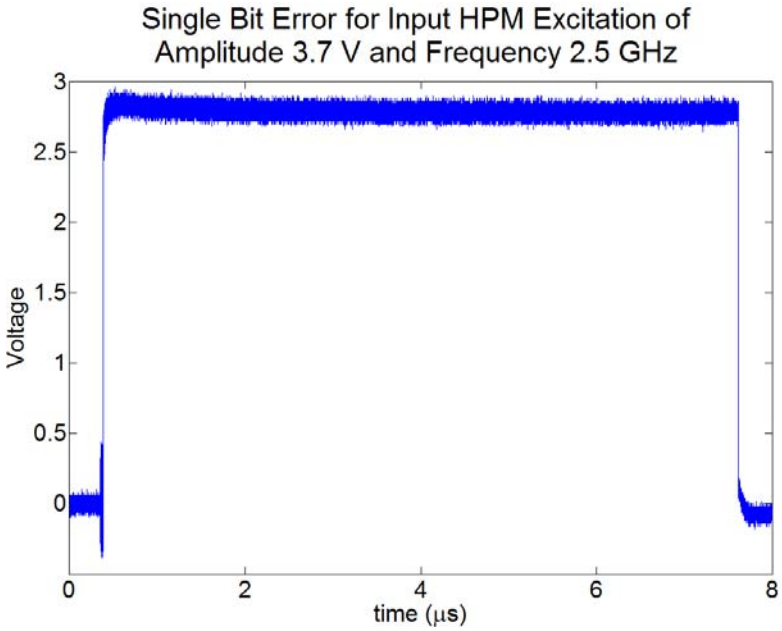

Figure 5.25: Example of single bit error in the inverter chain test circuit

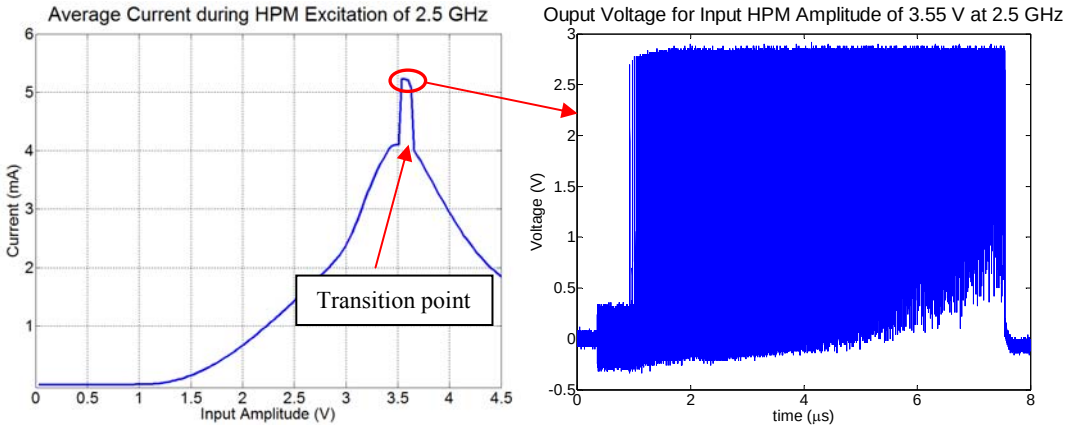

Figure 5.26: Current measurement for the inverter chain circuit with input drive of 2.5 GHz (left); Output voltage during current spike at 2 V input amplitude (right)

The interesting feature from the plots to consider is that the current does not appear to correspond to the behavior of output voltage. The theory presented in section 5.3.2 suggests that in the case of full state changes, current is only drawn

during the voltage transitions. However, the current behavior demonstrates similar characteristics to the current of the single inverter at the same frequency as presented in section 5.2. For the single inverter it was shown that the input detected voltage will bias the device into conduction as the HPM amplitude increases. The current behavior of the inverter chain is likely due to the similar situation. The input buffer, which is constructed by two of the single inverters from the previous section, will experience the same input bias conditions as the single inverter test circuit. Once the DC bias level reaches the transitional region of the first buffer's voltage transfer curve, the output DC level will shift and change the input bias of the next device. In essence the DC bias will cascade through the first stage and potentially bias other stages of the circuit into conduction regions of their transfer characteristics. Ignoring the current spike for the moment, the peak current is approximately 4 mA, and it occurs at the RF amplitude of 3.5 V. Recall from figure 5.16 that at the same drive frequency, the input detected voltage and mean output voltage of the single inverter were both approximately 1.5 V. For the inverter chain circuit, both inverters of the buffer stage are therefore biased at the point of peak conduction. The fact that the measured peak average current is twice the peak current present in the DC current transfer curve in figure 5.17 also supports this conclusion. The dynamic gain of the circuit increases with each successive inverter, similar to what was demonstrated for the output buffer circuit in figure 2.19. Therefore the likelihood of later stages beyond the input buffer being biased is minimal, since voltage transitions in later stages will be very abrupt. Any dynamic current component will also be very small since the load capacitance of the input buffer is on the order of 10's of fF.

Notice the short current spike that occurs between input drive amplitudes of 3.5 V and 3.6 V in figure 5.26. To the right of the current plot is the output voltage waveform associated with the input drive amplitude of 3.55 V, where the current spike occurs. The output voltage shows spurious oscillations within this small window of input amplitudes. This type of oscillation will be discussed in detail shortly, but the full and rapid switching of the output stage at this point increases the dynamic component of the total current causing the spike to occur. Once the circuit settles into the output state shown in figure 5.25, the current resumes its original behavior.

The second out-of-band effect observed is spurious voltage oscillations at the output of test circuits. These oscillations always occur at frequencies lower than the input HPM frequency. Figure 5.27 is a spectrogram of the output voltage for the inverter chain circuit when the input is excited by a 1 GHz RF signal. The color map is in log scale in order to better visualize the spectral lines. At approximately 5 V amplitude, notice the onset of oscillations. The enlarged portion of the graph shows the dominant frequency of 34.4 MHz along with many visible harmonics. This frequency also mixes with the fundamental frequency, which is evident from the spectral lines spaced 34.4 MHz apart around the 1 GHz line.

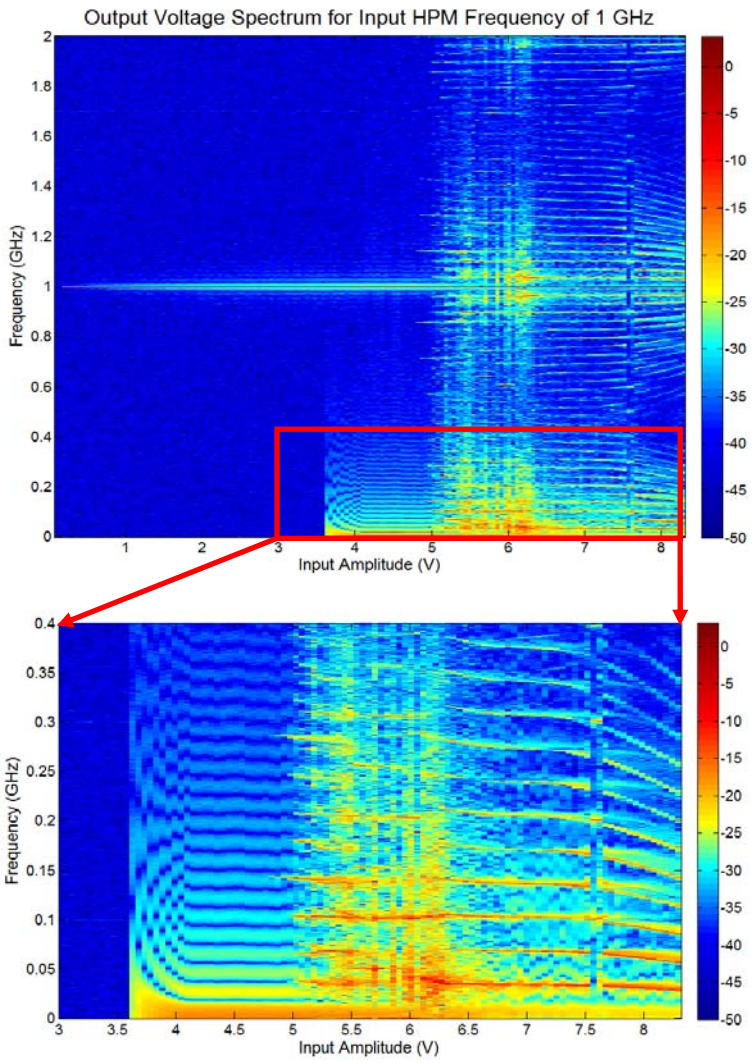

Figure 5.27: Output voltage spectrum for the inverter chain test circuit with RF input frequency of 1 GHz

There are some interesting features highlighted by the spectral plots. First look at the enlarged portion for input amplitude of 6 V. For a significant portion of this part of the plot there is no dominant frequency in contrast to larger amplitudes where there is a well defined spectral line at 34.4 MHz. To get a better picture of what the output waveform looks like for both these conditions examine the plots in figure 5.28.

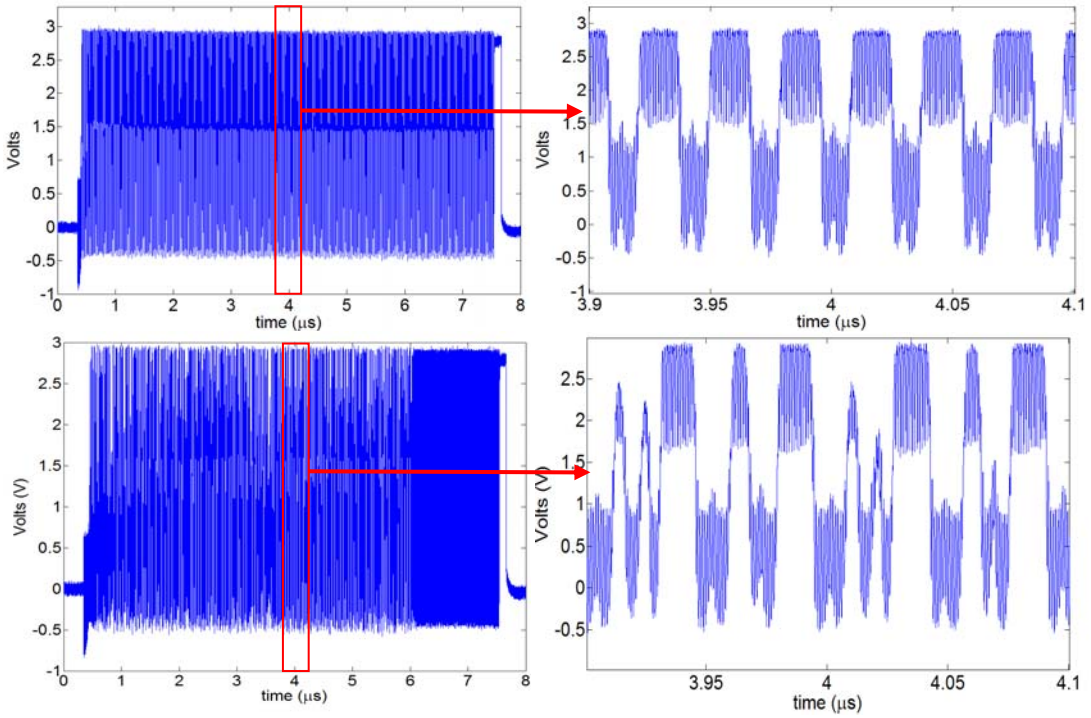

Figure 5.28: Example of stable (top) and aperiodic (bottom) output oscillations for the inverter chain test circuit driven at RF frequency of 1 GHz

The top waveform in figure 5.24 shows a stable periodic output oscillation that occurs for the duration of the HPM pulse. The state changes occur at a constant frequency of 34.4 MHz with high frequency components superimposed on the signal. The periodic oscillations also appear to be phase locked with the input drive signal. The bottom output waveform is for input amplitude of 6 V and demonstrates aperiodic state changes, which do not appear to have any periodic structure throughout the duration of the HPM excitation. Another interesting feature is the how the spectral lines curve slightly as the input amplitude changes. This suggests that there is a resonance tuning associated with this effect that is a function of the input amplitude. Figure 5.31 shows the same phenomena occurring in the flip-flop circuit, and figures 5.32 - 5.35 show

the output spectrum for each of the bits of the four bit counter from least significant bit to most significant bit.

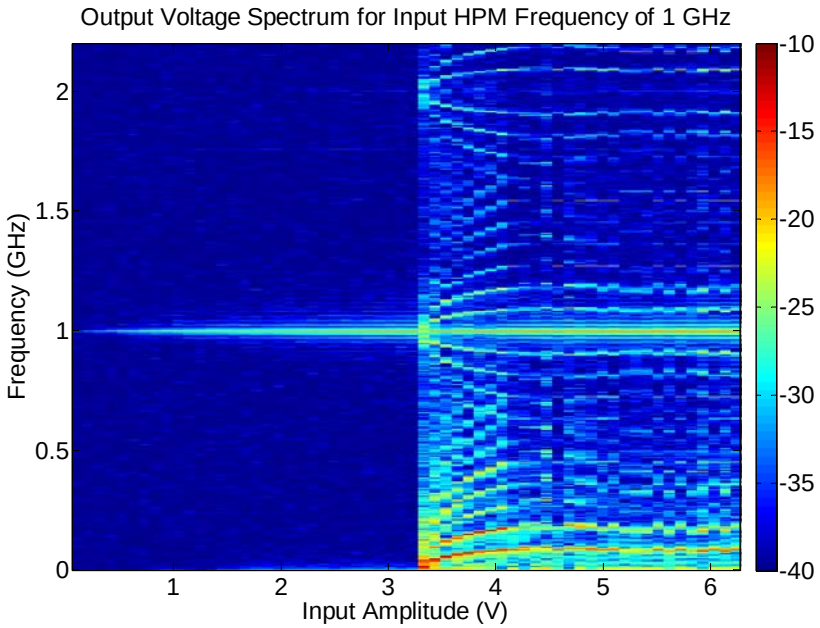

Figure 5.29: Output voltage spectrum for the flip-flop test circuit with RF input frequency of 1 GHz.

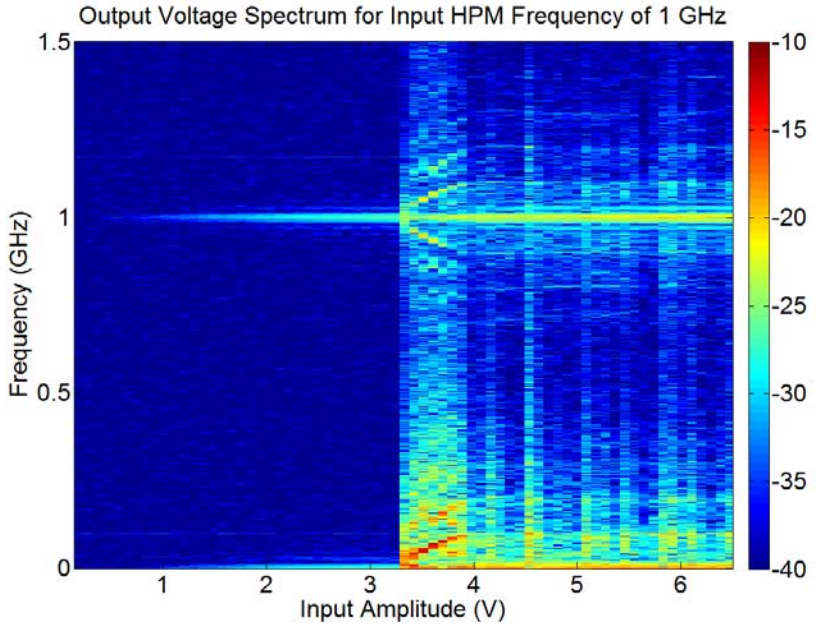

Figure 5.30: Output voltage spectrum for the least significant bit of the counter test circuit with RF input frequency of 1 GHz.

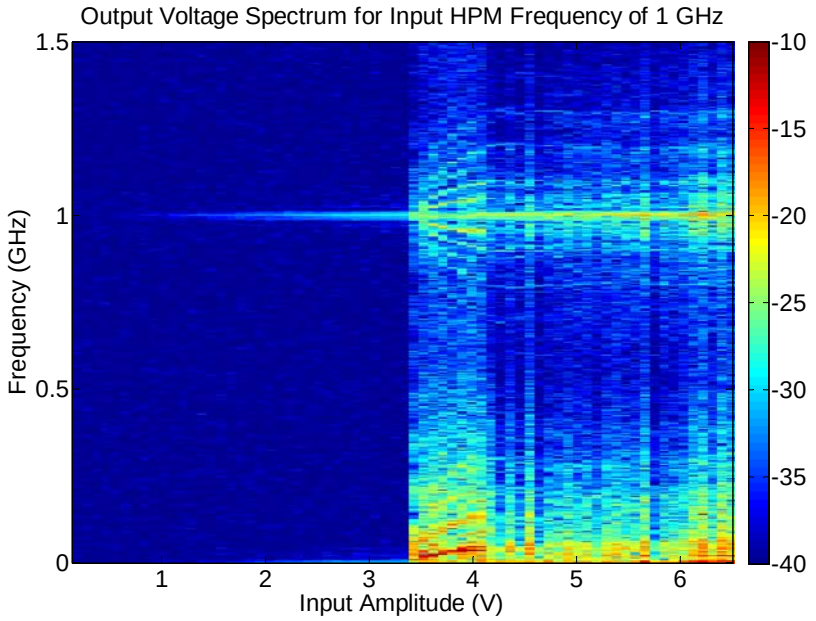

Figure 5.31: Output voltage spectrum for the second least significant bit of the counter test circuit with RF input frequency of 1 GHz.

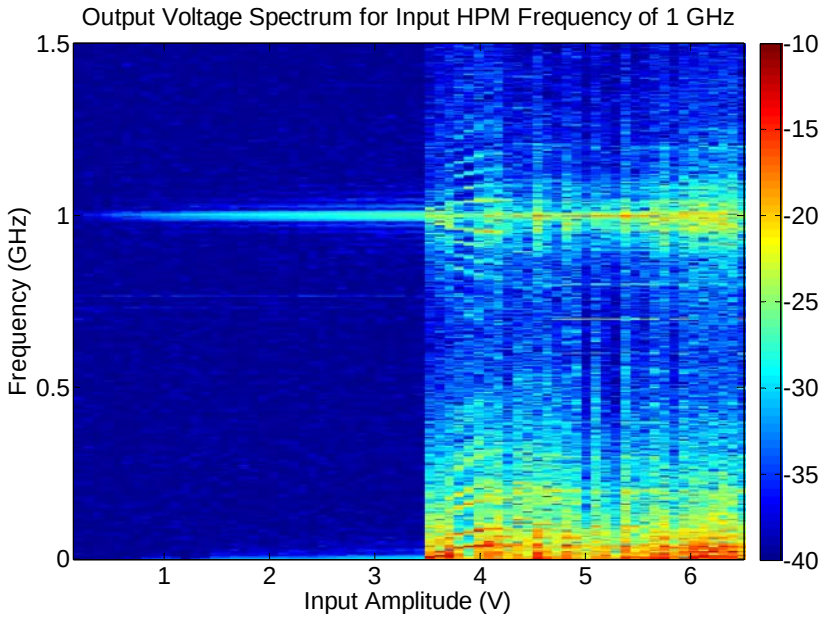

Figure 5.32: Output voltage spectrum for the second most significant bit of the counter test circuit with RF input frequency of 1 GHz.

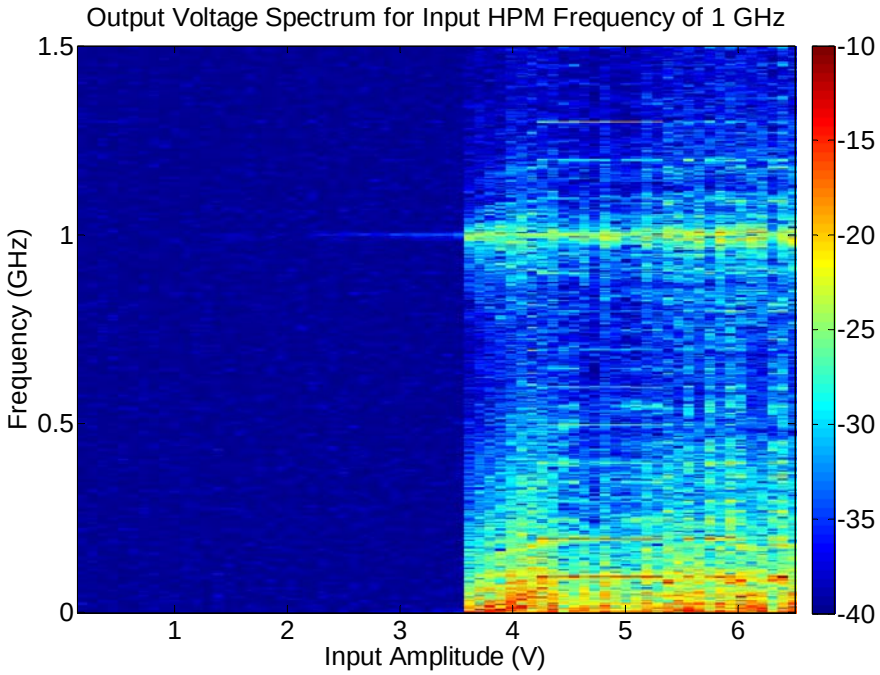

Figure 5.33: Output voltage spectrum for the second most significant bit of the counter test circuit with RF input frequency of 1 GHz.

The output voltage behavior of the JK flip-flop also demonstrates periodic oscillations that appear to be phase locked with the input of the drive signal for a drive frequency of 1 GHz. In contrast, the output voltages of each of the bits of the counter demonstrate aperiodic oscillations. For the counter, this is true at every test frequency measured in these experiments, which suggests that the periodic oscillations are less likely to occur in more complex circuits.

Figures 5.32 - 5.34 show the average current measured for each test circuit as the circuit was excited by a 1 GHz HPM signal. Notice that current behavior resembles the behavior of the single bit error in figure 5.26 up to the threshold of the output oscillations. Once the oscillations occur the average current approximately doubled for each of the test circuits. It is reasonable to assume, based on the analysis presented previously in this chapter that the increased current is due an increase of the

dynamic current caused by the output stage switching state while driving he output capacitance.

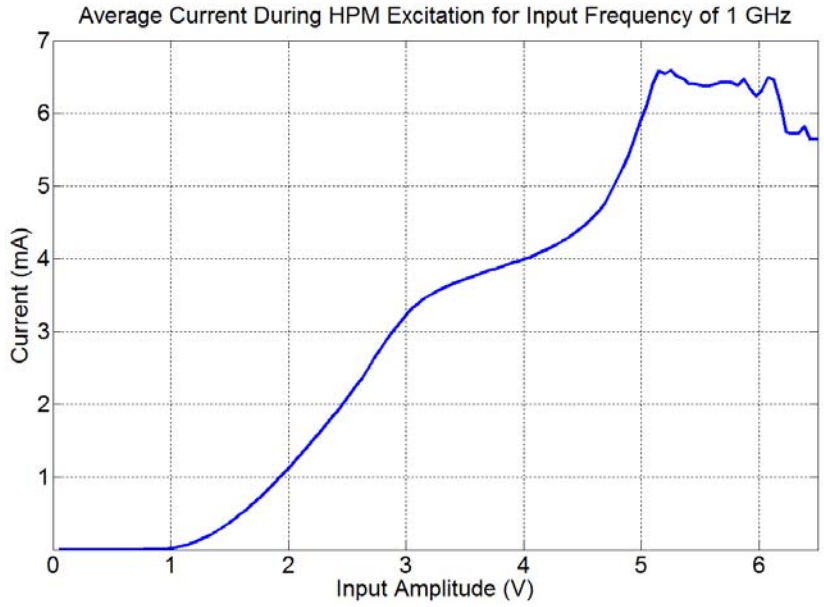

Figure 5.34: Current measurement for the inverter chain test circuit with an input RF frequency of 1 GHz

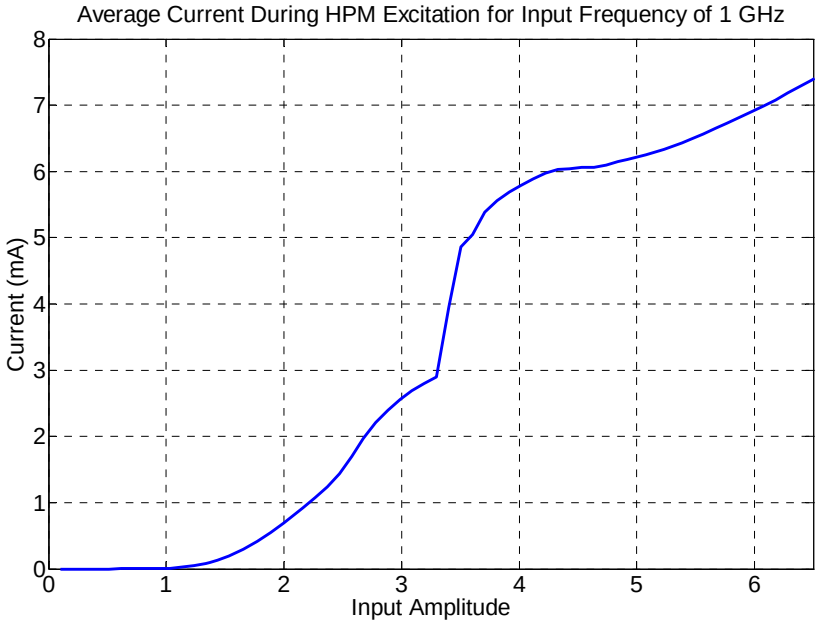

Figure 5.35: Current measurement for the JK flip-flop test circuit with an input RF frequency of 1 GHz

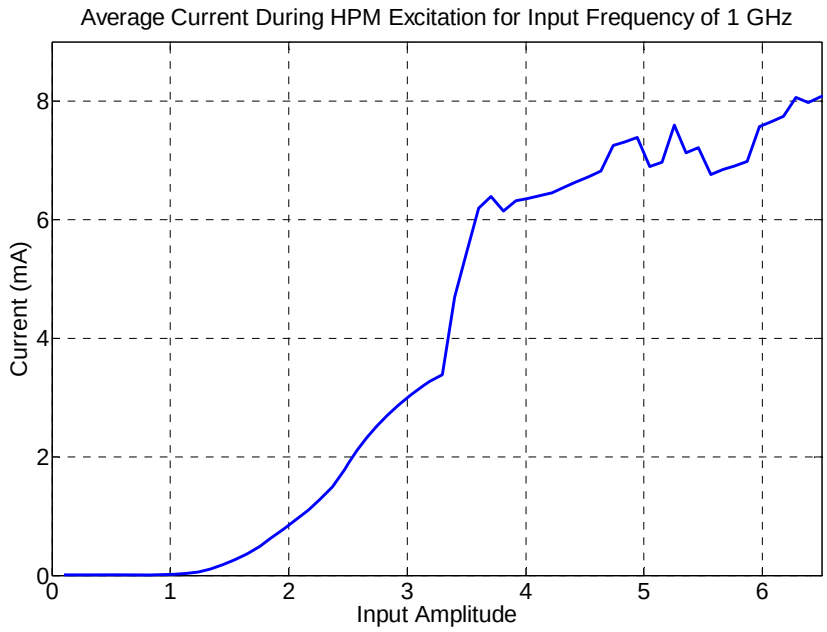

Figure 5.36: Current measurement for the 4 bit counter test circuit with an input RF frequency of 1 GHz

The local by-pass capacitor should ensure that the impedance of the power supply, picoameter, and cables are not introducing parasitic elements that produce this effect. However, to ensure that the effect is not a result of these elements, the same experiment, minus current measurements, was performed with the lithium ion battery attachment that was described in Chapter 3. The behavior of the test circuits using the battery power was precisely the same as the behavior when using the power supply.

5.4.3 Analysis of Out-of-Band Oscillation Effects

The hypothesis for the cause of the occurrence of the spurious oscillations is that there is a feedback mechanism being driven by the HPM signal. The following section presents experimental evidence and analysis to support this hypothesis. The case of stable oscillations in the inverter chain circuit are examined in order

understand the dynamics of this phenomenon. In all instances of the stable phenomenon occurring, the oscillation frequency at the output is almost exactly a sub-harmonic of the RF input frequency and the output oscillations appear to be locked in phase with the input signal. For instance, in the data presented in figure 5.27 for the inverter chain circuit, the output oscillation frequency of 34.4 MHz is the 29^{th} sub-harmonic of 1 GHz.

One likely feedback path from the output to the input is through the V_{dd} line and ggPMOS to the input of the circuit. The dynamic capacitance of the ggPMOS and the parasitic inductance of the board trace elements and ball bond wire would form a resonant structure. The resonance is excited by the current fluctuations that occur on the power line as the input signal drives the circuit. Due to circuit nonlinearities, the resonant frequency and the fundamental drive frequency mix to create a difference frequency or beat frequency on the power line that appears as an envelope to the V_{dd} voltage fluctuations. For example, in the case of the data presented in figure 5.27, the resonance (or harmonic of the resonance) of the feedback would be approximately 1034 MHz, thereby creating a beat frequency of 34 MHz. When the beat frequency is at a minimum, V_{dd} would be lowered and the voltage needed to switch the state of the CMOS inverter is also effectively lowered. The state changes would occur when the input voltage signal is high at the same time V_{dd} voltage is low. When the beat frequency is close enough to a sub-harmonic of the input drive frequency then the state changes occur periodically in phase and hence the phase locking phenomenon.

Figure 5.29 are the FFT's of the recorded output and input signals of the inverter chain circuit for input drive amplitude of 6.5 V at 1 GHz.

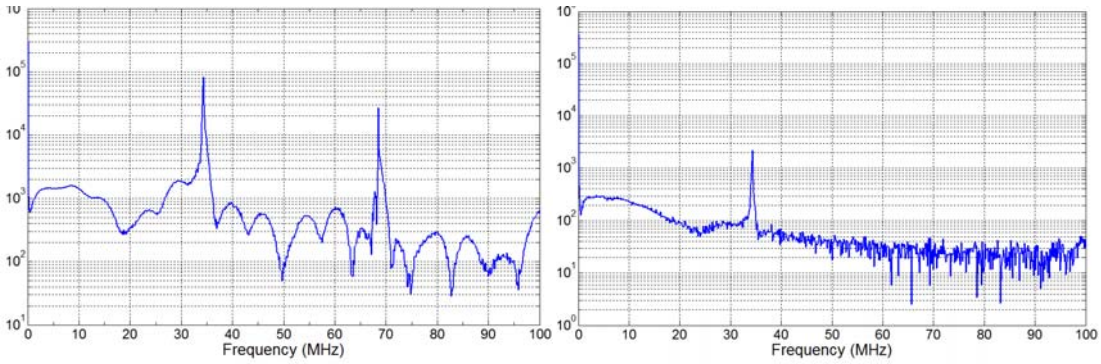

Figure 5.37: Lower band frequency spectrum for the output (left) and the input (right) for an input RF amplitude of 6.5 V at 1 GHz

A 34.4 MHz component on the input is clearly visible in figure 5.25, which demonstrates feedback. The magnitude of this component is attenuated due to the series resistance in the bias circuit as described in Chapter 3.

Consider the following analysis, which examines the phase correlation between the output signal and the input signal. It is logical to assume that V_{dd} fluctuations due to parasitic inductance are π out of phase with the output voltage. As the output voltage switches from low to high state, current is drawn from the supply to charge the output capacitance. Parasitic inductances of the V_{dd} line will oppose the change in current and the net voltage on the power line lowers. To examine the phase correlation of the output and the input voltage, the phase versus time was calculated for both the input and output waveforms of the inverter chain circuit using the Hilbert transform (eq. 5.12 and 5.13) [60]. The measured data used in the analysis is for an HPM frequency of 1 GHz and input amplitude of 6.5 V.

$$y(t) = \frac{1}{\pi}\int_{-\infty}^{+\infty}\frac{x(\tau)}{t-\tau}d\tau \tag{5.8}$$

$$\phi(t) = \tan^{-1}\left(\frac{\mathrm{Im}[y(t)]}{\mathrm{Re}[y(t)]}\right) \tag{5.9}$$

The phase difference between the input and the output as a function of time is plotted in figure 5.30 (red) along with the output signal (blue).

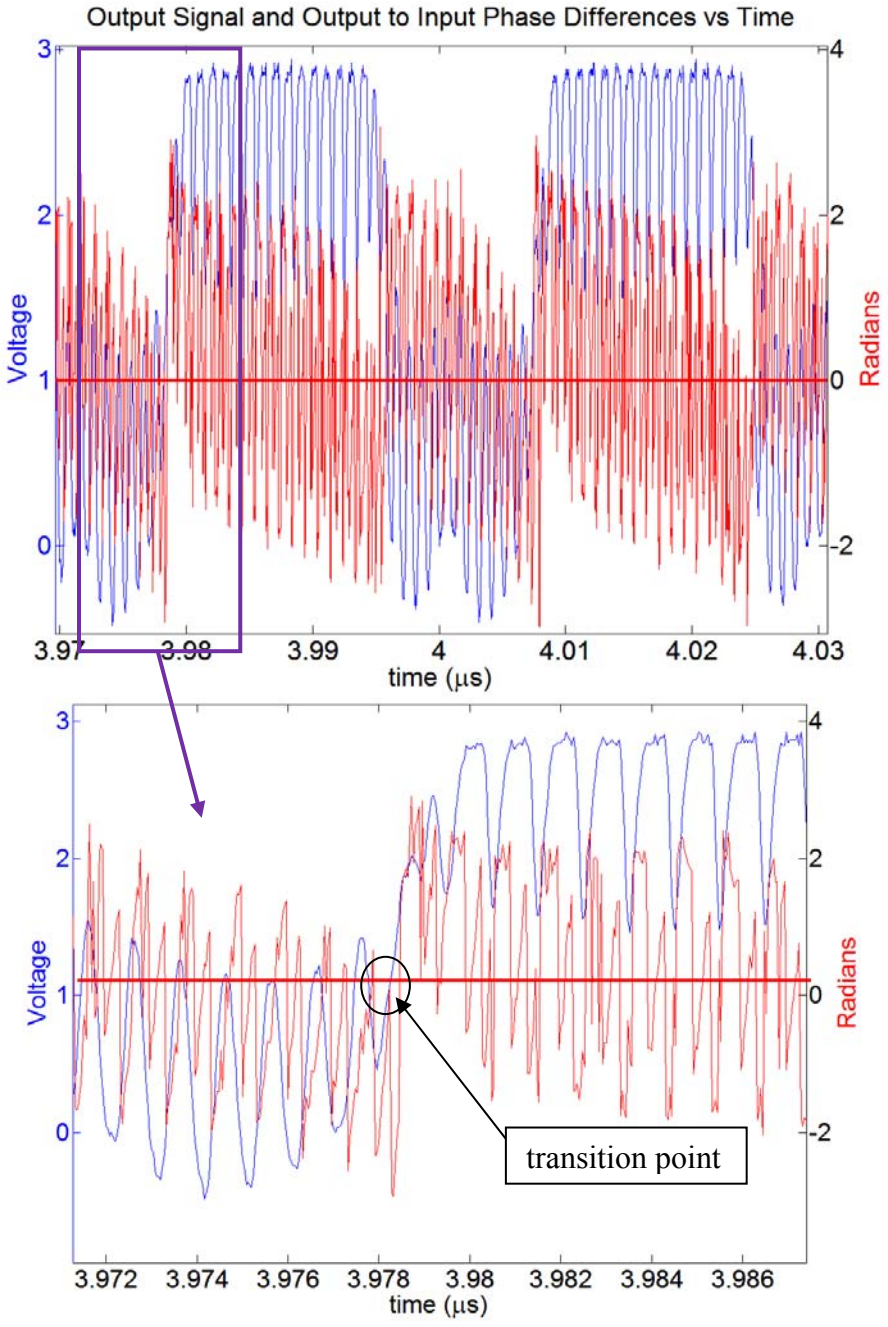

Figure 5.38: Plot of the input and output voltage phase difference compared to the output signal. The output signal trace is blue and the phase difference is red.

The phase of each signal, as represented in the plot, varies with time from $-\pi/2$ to $+\pi/2$ at which point a jump discontinuity occurs and the cycle repeats. As a result of subtracting the phases, the faster cycle on the phase curve, due to the input signal, is superimposed on the slower moving phase of the output. In the bottom plot of figure 5.30, notice that at the state transition of the output signal from low to high, the phase difference is zero at the point when the faster moving phase of the input is at $\pi/2$. This means that the output phase is also $\pi/2$ and therefore the voltage phase of the power line is at $-\pi/2$. In terms of voltage amplitude, this means that the input voltage is at its maximum when the voltage of V_{dd} is at its minimum. This proves that the periodic output oscillations observed are in fact phase locked with the input signal. This also presents strong evidence that supports the hypothesis that the observed oscillations are the result of the nonlinear dynamics that occur due to a feedback mechanism. The fluctuations of the power line create conditions that allow the output to switch state depending on the voltage at the input at a given time. Assuming that the hypothesis is correct than the tuning effect apparent in the spectral lines as the input amplitude increase is likely due to the dynamic capacitance of the ggPMOS. In the NQS regime, there is always some average amount of excess minority carriers present in the drain-body diode of the ggPMOS, which contributes to the diffusion capacitance. As the amplitude of the input further exceeds V_{dd}, the average value of minority carriers will increase, affecting the total capacitance of the device and therefore tuning the resonance of the feedback path.

5.5 Summary and discussion

In this chapter the various HPM effects observed in experiment were presented as well as analysis of the circuit dynamics that produce these effects. The following charts were made to summarize all of the experimental observations based on the behavior of the output voltage waveform and the HPM voltage amplitude at the input terminal of each circuit. The charts map 4 distinctions in the circuit behavior defined by the color legend in Figure 5.39. The label "No effect" is defined as the output voltage displaying no amplitude that exceeds the noise margin of input buffer to a hypothetical connected device. A conservative value of 1.2 V is chosen as the threshold noise margin based on the noise margins of the logic devices and buffer circuits presented in Chapter 2. The blue region labeled "In-Band Oscillations" refers to the effects observed where the HPM causes state switching at the same frequency as the HPM signal. In these cases it was observed that the quasi-static approximation is valid, and the input signal is rectified. When the amplitude exceeds the rail voltage the waveform takes the shape of a normal logic signal. The region labeled "Single Bit Error" refers to the case where the output produces a single state change when excited by HPM. For the inverter chain circuit this manifested as a single square pulse with a pulse width equal to the width of the HPM pulse. For the flip flop and counter circuits, this usually resulted in a state change at either edge of the HPM pulse. The region labeled "Nonlinear Dynamics" refers to state oscillations of the output at frequencies lower than the HPM frequency. As was demonstrated by the preceding analysis this behavior is most likely influenced by a feedback mechanism through the V_{dd} line and the ESD protection device. This classification includes both

the phase-locked phenomenon and aperiodic oscillations reported in section 5.4.2. The region labeled "Out of Experimental Range" represents input voltage amplitudes that were not attainable for input power levels from -20 dBm to 20 dBm. The input amplitudes are based on the input gain measurements presented in Chapter 4.

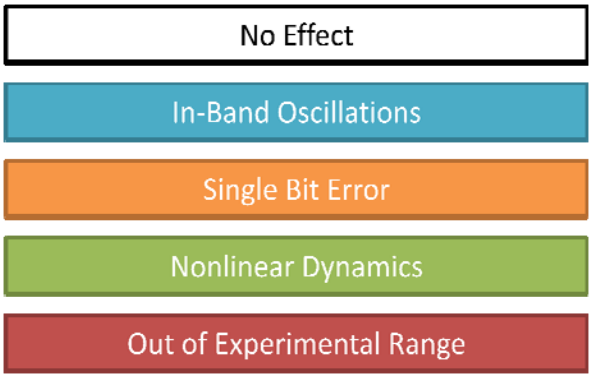

Figure 5.39: Color legend for the summary of results presented in figures 5.40, 5.41, and 5.42

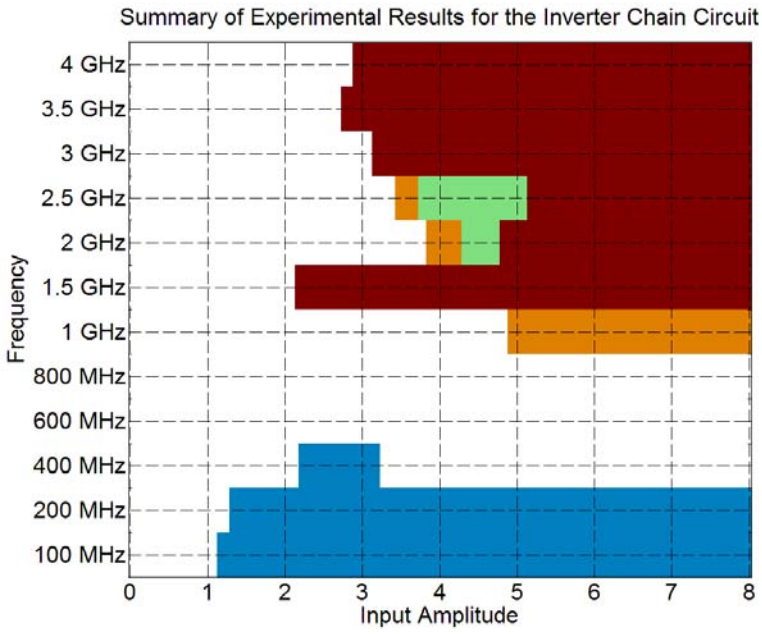

Figure 5.40: Summary of effects observed for the inverter chain circuit

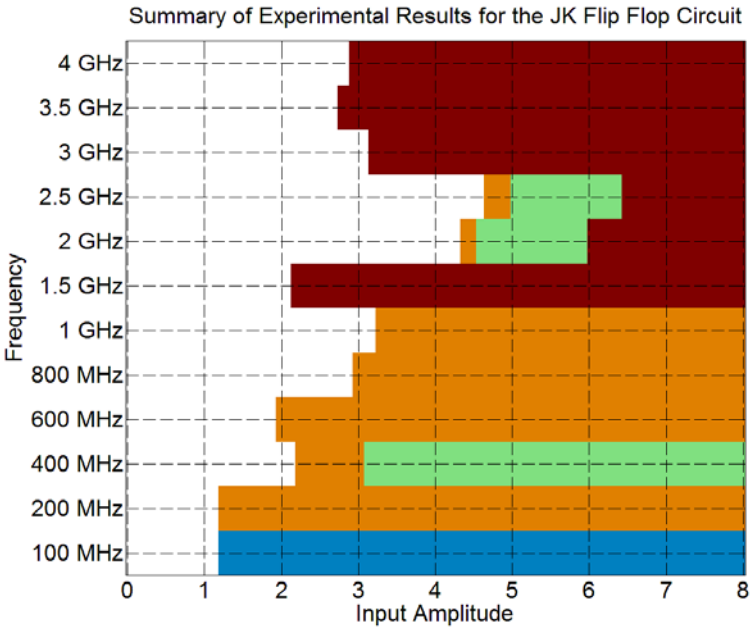

Figure 5.41: Summary of effects observed for the JK flip flop circuit

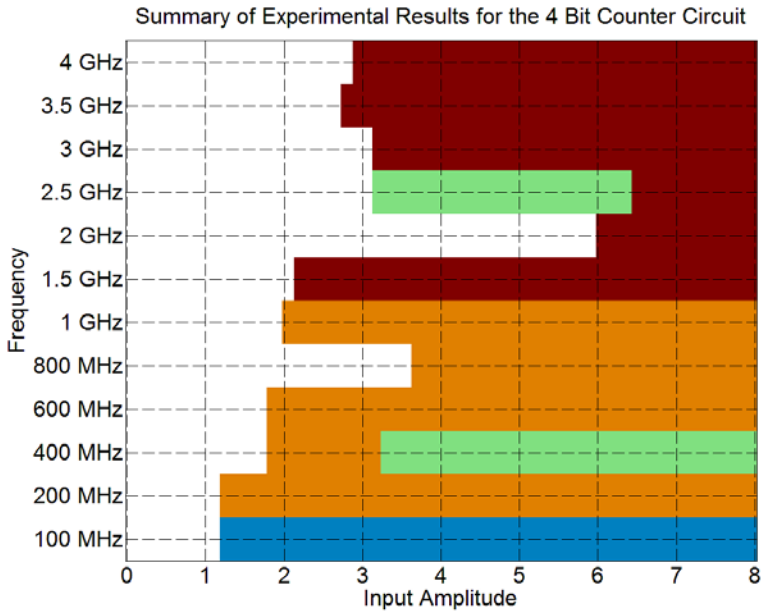

Figure 5.42: Summary of effects observed for the 4-bit counter

It was demonstrated that the maximum switching speed of a CMOS digital circuits is an influential characteristic in HPM effects. At frequencies below the maximum switching speed, HPM singnals will produce multiple bit errors that are synchronized to the HPM excitation frequency. Results from theoritcal analysis show that current draw induced by HPM signals is predicted by established CMOS thoery. Out-of-band HPM excitations produced two catagories of effects. Single state changes occur as the input DC bias increases due to the nonlinear response of the ESD devices. The current draw for frequencies where single state changes occur is dominated by short circuit current due to the input detected voltage biasing the input buffer inverters into conduction. Spurious voltage oscillation at frquencies much lower than the input drive frequency were also observed at the output of the test circuits for out-of-band frequencies. The voltage oscillations demonstrated both periodic and aperiodic characteristic for different drive frequencies and amplitude. Results of anlysis show that spurios oscillations are likely caused by a feeback mechanism through the V_{dd} line and the ESD protection device at the input of the circuit. Current draw during instances of spurious oscillations is a combination of short circuit current produced by DC bias at the input buffer and dynamic current produced by the state switching at the output.

In general it has been shown that HPM signals are capable of producing a large amount of bit errors to a system, which could potentially cause system upset. Particularly susceptible would be any systems that rely on previously stored states from registers or memories. HPM interference could potentially introduce an enormous amount of asynchronous bit errors that can scramble stored information.

Also, HPM may cause abnormal current levels in a system that could potentially lead to upsets events such as triggering fault protection devices. In the particular case of spurious oscillations, the average current reached levels as much as three times that measured at the maximum operating frequency of the devices under normal digital excitation. If such effects are stimulated at multiple ports of larger systems, the current spike could potentially be excessive enough to harm the system.

Chapter 6 : Modeling HPM Effects in CMOS

6.1 Modeling Approach

An important goal of this work is the modeling of HPM effects in devices and circuits. Modeling HPM effects on current technology is very challenging, especially as devices have become smaller. Short channel effects in MOSFET transistors such as source-drain charge sharing, drain induced barrier lowering, and subsurface punch through continually have a pronounced effect on important parameters such as threshold voltage and leakage currents, which decrease noise margins and increase power consumption [44, 52]. As frequencies become higher parasitic impedances have a much greater influence on circuit performance [61-63]. The modeling of HPM effects benefits a great deal from the continuing research and development of models to meet the contemporary challenges. However, there are aspects of HPM effects that may profoundly challenge current analytical techniques. HPM signals have high frequencies and are potentially very high amplitude. In many circumstances HPM can excite amplitudes on board traces that exceed the rail voltages of the system components as was studied in the previous two chapters. These large voltages can drive nonlinear circuit behavior and forward bias junctions that would other remain reverse biased during normal circuit operation.

There are two general approaches to developing circuit models, which are equivalent circuit models[63, 64] and compact models[65-67]. Equivalent circuit modeling methods use lumped elements such as charge and current sources in addition to basic analytical device models to account for additional circuit behavior under various conditions such as high frequency or large signal inputs. The

parameters for the various elements are acquired through I-V characterization, C-V measurements, and S-parameter extraction[63]. The advantage of equivalent circuits is that they tend to be accurate with a fairly small number of parameters, and the extraction of these parameters is fairly simple. The simplicity of this method allows for more freedom to address specific conditions. The disadvantage is that the model is not scalable and the parameter extraction is only valid for the measured device.

Compact models are the most widely used analytical models in the IC circuit design and fabrication industry. The model parameters are also extracted from DC I-V curves, C-V measurements, and S-parameter analysis, similar to equivalent circuits but this process is far more complex than equivalent circuit method discussed above. The difference with compact models is that parameters are extracted from numerous devices with various gate lengths and widths. The parameters are calculated from the measurements using commercial software such as Agilent's IC-CAP (Integrated Circuit Capture and Analysis Program). Individual integrated circuit foundries such as IBM or On Semiconductor fabricate test wafers and provide the compact model parameters for their customers. One advantage of compact models is that they are scalable, which makes circuit design easier. Another advantage is that compact models such as BSIM (Berkeley Short-channel IGFET Model) have become industry standards[65]. Even though there are hundreds of parameters for compact models, they are relatively easily obtained from the foundry for a given process. Almost all commercial IC design and simulation software packages support compact models. The disadvantage of compact models is that their analytical expressions are complex with large numbers of parameters [66, 67]. Altering them to accommodate for

extreme operating conditions is more difficult than with equivalent circuits.

The compact model BSIM4 is used in the modeling efforts presented in this work since they are the most widely used compact model in industry for digital CMOS design [65]. For HPM effects modeling to be the most useful, the modeling methods should be easily incorporated into the design cycle. The idea is that this will facilitate susceptibility analysis and countermeasure design during the design phase and potentially decrease the cost of HPM evaluation process a great deal.

Agilent ADS (Advanced Design Systems) is the circuit simulator used for effects modeling in this work. ADS has a large variety of useful features for high frequency circuit simulation such as transient analysis, harmonic balance, and S-parameter analysis. ADS also has the ability to incorporate an S-parameter based linear models for things such as trace and ball bond wire impedances, which allows for more accurate analysis across a large range of frequencies as opposed to estimating circuit traces with lump element equivalents.

The following chapter presents techniques which use BSIM compact model for simulating HPM effects. There are two contexts for the level of accuracy required to predict circuit performance when excited by HPM signals. First is the ability to predict effects threshold for a given terminal voltage. Exact reproduction of circuit behavior is not necessary for the purpose of determining effects thresholds. For example, if for a given circuit an effect in the form of bit errors occurs for particular input voltage amplitude, then the model only needs to predict where the onset occurs within a few percent of input voltage amplitude. The nature and severity of the effect seen on the output waveform is not as important.

The second important context is the modeling effects to aid in the design and testing of HPM countermeasures. As researchers explore more effective means to counter HPM effect beyond just shielding, modeling techniques will be invaluable. For this context, accurate prediction of circuit behavior is far more important especially if the countermeasure itself is an electronics device or circuit design technique. Therefore it is beneficial for both situations to endeavor to model HPM effects with as much accuracy as possible and to determine how accuracy can be improved.

6.2 Modeling the Input ESD Response to HPM Excitation

This section covers the results of the modeling efforts with respect to the ESD response. The first sub-section will cover the background on how BSIM calculates drain/source to body PN junction capacitance and current, and how it pertains to modeling HPM effects. The later part of the section presents a method for improving upon the accuracy of BSIM and compares the simulation results to the measurements for the input response reported in Chapter 4.

6.2.1 Background on BSIM Drain/Source to Body PN Junction Model

The drain bulk PN junction is the most relevant region of the ESD protection devices used in the test circuits. The analytical expression BSIM4 uses to calculate the drain source current is given by equation 6.1[67].

$$I_{bd} = I_{sbd}\left[\exp\left(\frac{qV_{bd}}{NJD \cdot k_B TNOM}\right)\right] + V_{bd}G_{\min} \tag{6.1}$$

I_{sbd} is the saturation current, which is calculated from layout dimensions and extracted BSIM parameters[67]. *NJD* is the junction emission coefficient , *TNOM* is the temperature at which the device parameters were extracted, and k_B is Boltzmann's constant. G_{min} is a small conductance that circuit simulators add across nonlinear devices to prevent nodes from floating if the device is completely turned off.

The drain bulk diode capacitance is the sum of three capacitances based on the geometry of the drain region given by equation (6.2).

$$C_{bd} = A_{deff} C_{jdb} + P_{deff} C_{jdbsw} + W_{effcj} \cdot NF \cdot C_{jbdswg} \tag{6.2}$$

C_{jbd} is the bottom junction capacitance per unit area, C_{jdbsw} is the unit area junction capacitance along the drain sidewall on the isolation side, and C_{jbdswg} is the sidewall unit area junction capacitance on the gate side. $A_{deff,}$ P_{deff}, and W_{effcj}, are respective area parameters and *NF* is the number of device fingers. Each of the capacitances is calculated using one of the following two equations, depending on the value of the voltage across the junction, V_{bd}.

$$C_{jbd} = CJD \cdot \left(1 + MJD \cdot \frac{V_{bd}}{PBD} \right) \tag{6.3}$$

$$C_{jbd} = CJD \left(1 - \frac{V_{bd}}{PBD} \right)^{-MJD} \tag{6.4}$$

Equation (6.3) is used when V_{bd} is greater than zero and the junction approaches and exceeds forward biased. When V_{bd} is less than zero and the junction is reverse biased, equation (6.4) is used to calculate the junction capacitance. CJD is the zero bias junction capacitance value, PBD is the built in sidewall potential, and MJD is the capacitance grating coefficient. The equations for the other two capacitances in equation (6.2) are the same but with the appropriate equivalent BSIM parameters

used for each one. For C_{jdbsw} the parameters are CJSWD, PBSWD, and MJSWD, and for C_{jbdswg} the parameters are CJSWGD, PBSWGD, and MJSWGD. Both the equation for the current and the capacitance are basic and lack vital physical parameters that would greatly aid in HPM modeling. Both equations are exclusively quasi-static, since there is no time dependence on the junction voltage within the device. Also, there is no accounting for the excess minority carrier (diffusion) charge in the bulk when the diode is forward biased, and hence there is no calculation of the contribution of diffusion capacitance to the total capacitance in the forward bias regime[65]. When the junction is reverse biased or at zero bias the model is accurate. However, as was demonstrated in figure 4.16, when the ESD devices are forward biased the total capacitance increases exponentially and can be a few orders of magnitude larger than the reverse bias conditions due to the diffusion capacitance [51, 52]. The reason BSIM has such limited analytical models for PN junctions is because under almost all normal operating conditions of CMOS circuits, the PN junction will be reversed biased, and the simple analytical expressions it uses are adequate for the intended use of the model[65]. This is done to eliminate additional unnecessary computations from simulations [65].

6.2.2 Compensating for Non Quasi-Static Behavior

The previous two chapters have demonstrated that the ESD protection devices contribute significantly to HPM effects in the test circuits. At high frequencies these devices enter the NQS regime and junction transients are essential to modeling the ESD behavior. BSIM intrinsically is incapable of accurately modeling NQS behavior in PN junctions. To overcome this difficulty a substrate resistor network is used to

create a time constant with the diode capacitance to account for the junction voltage time dependence.

A substrate resistor network has often been implemented as part of a model for improving RF integrated circuit simulation of MOS transistors [61-63]. The network is meant to account for signal coupling through the substrate. One of the improvements of BSIM 4 over its predecessor, BSIM 3v3, is the incorporation of the resistor substrate network into the MOSFET model.

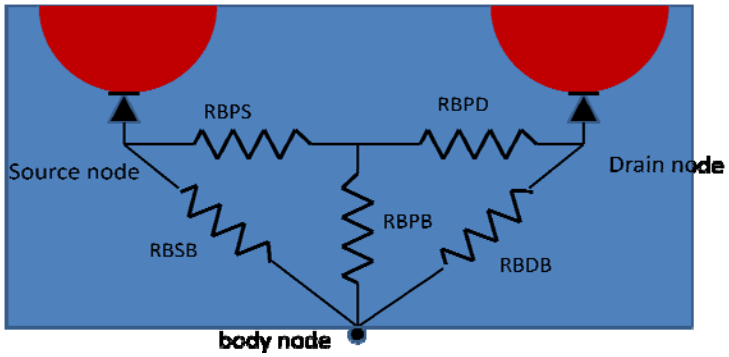

Figure 6.1: BSIM 4 substrate resistor network

The resistor network can be toggled on and off within the circuit simulator and the individual resistor values can be set for each individual MOSFET.

For the ESD devices, the source node and the body node are both connected to ground. For NQS modeling, the resistor between the drain and source and the drain and substrate are used in the ESD models. The time constant the resistor creates with the drain body junction capacitance is adjusted to model the effects of the reverse recovery time of the junction. As will be demonstrated, this method will improve the accuracy of the frequency response of the ESD protection devices with regard to the rectification efficiency, and the imbalance in DC response between the ggNMOS and the gcPMOS.

6.2.3 Input Response Simulations Results

This section presents the simulations results of the ESD response and demonstrates the improvement that the substrate resistance method contributes to the accuracy of the simulation. The simulations were performed using Agilent ADS with the circuit model shown in figure 6.2.

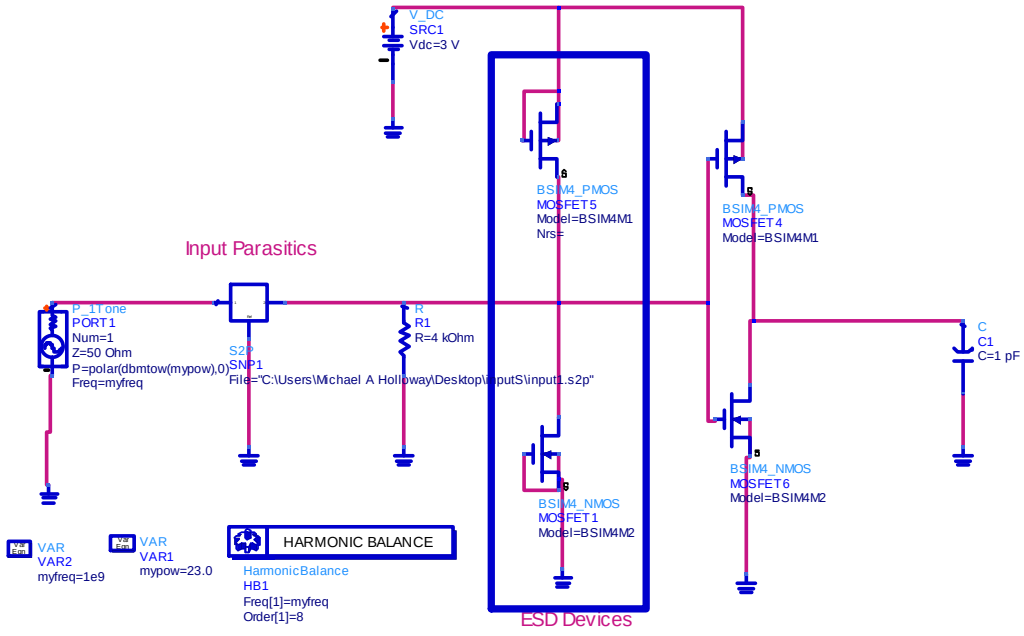

Figure 6.2: ADS schematic for input response simulation

In the schematic, notice the square element at the input labeled "Input Parasitics". This element contains the S-parameter measurements for the input parasitic elements presented in Chapter 4. This is a feature of ADS that allows the incorporation of linear elements in the form of S-parameters obtained though measurement or other simulation software.

The extracted BSIM parameters obtained from the foundry are entered into a BSIM 4 model element not shown in this figure. A complete list of all the parameters is given in the appendix. For each individual MOSFET the appropriate geometry

parameters obtained from the layout and given in Chapter 2 are entered. The 4 kΩ resistor between the input and ground represents the surface mount pull-down resistor present on the test circuit board.

The substrate resistor values for each of the ESD protection devices were adjusted to fit ESD response with measured experimental results. The total substrate resistor value between the drain body junction and ground for each of the ESD protection devices is given table 6.1.

Table 6.1: Substrate resistance value for the ESD protection devices

ESD Protection Device	*Substrate Resistance Value*
ggNMOS	75 Ω
gcPMOS	125 Ω

Simulations were performed using both transient analysis and harmonic balance analysis for comparison of each method. The advantage of harmonic balance is that the node voltages for all the linear elements are calculated in the frequency domain, while nonlinear elements are calculated in the time domain. By solving in the frequency domain, the steady state solution is calculated directly and only a single period of the input signal is needed. In contrast, transient analysis steps through many cycles of the drive signal before reaching steady state, which increases simulation time. Harmonic balance simulation is a significantly faster than transient; however, any interesting transient behavior will not be accurately simulated.

Figure 6.3 compares detected voltage predicted by simulation to the measured detected voltage at the input stage of the test circuits. The input drive was fixed to 15

dBm and the frequency was swept from 100 MHz to 4 GHz in steps of 10 MHz for both the transient and harmonic balance simulations.

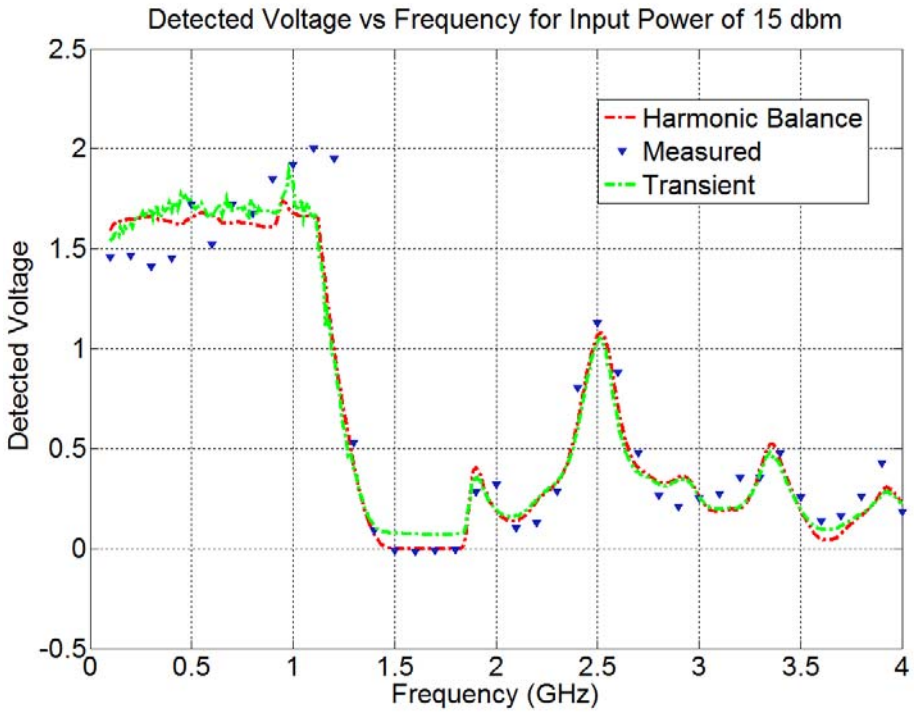

Figure 6.3: Comparison of simulation and experiment for the detected voltage of the ESD protection circuit at a fixed input power

The simulation curves show very good agreement with the measurements. The most noticeable deviation is in the range of 1.1 GHz and 1.3 GHz where the maximum deviation from the measured value is approximately 15%.

To examine the effectiveness of the ESD model more closely, observe figures 6.4 through 6.9. These plots are of simulation compared to measurement of the detected voltage versus input amplitude for 200 MHz, 1 GHz, and 2.5 GHz. Each frequency is plotted with a simulation that utilized the body resistance followed by a simulation without the body resistance.

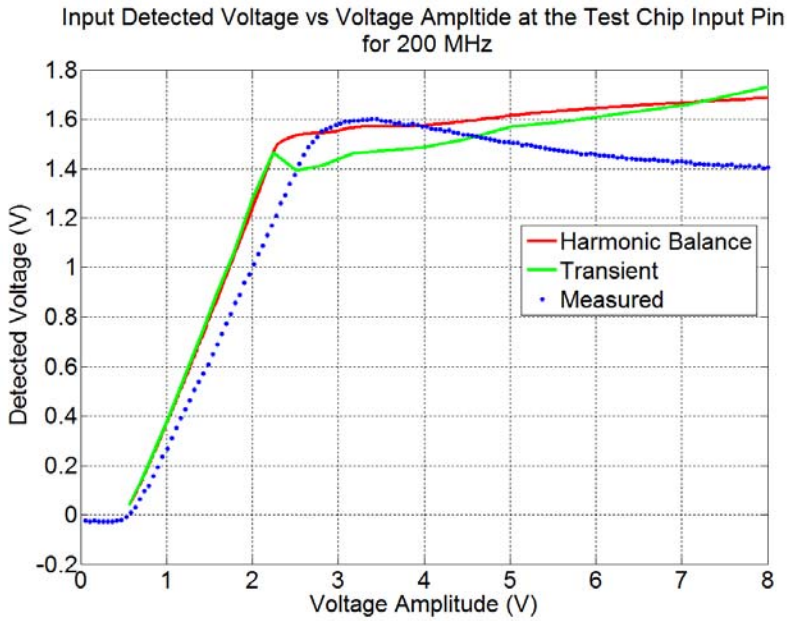

Figure 6.4: Detected voltage predicted by simulation with the body resistor ESD model vs. experiment for input frequency of 200 MHz

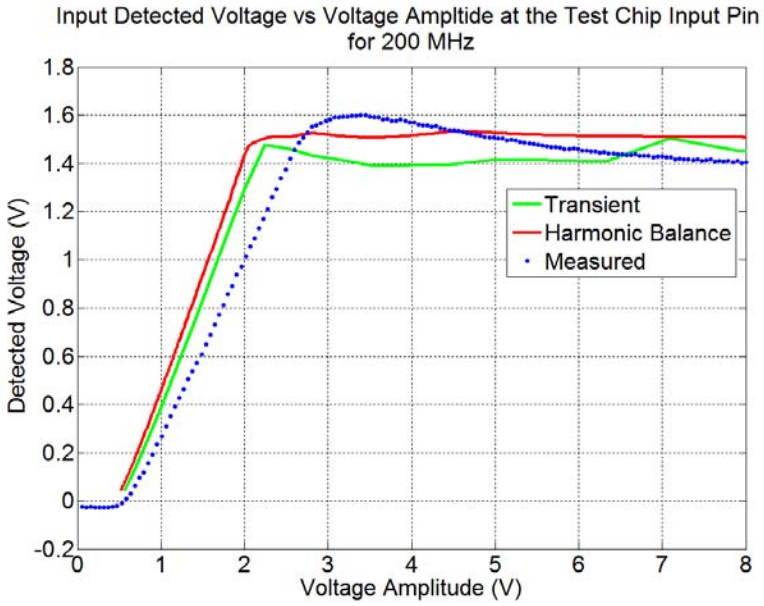

Figure 6.5: Detected voltage predicted by simulation without the body resistor ESD model vs. experiment for input frequency of 200 MHz

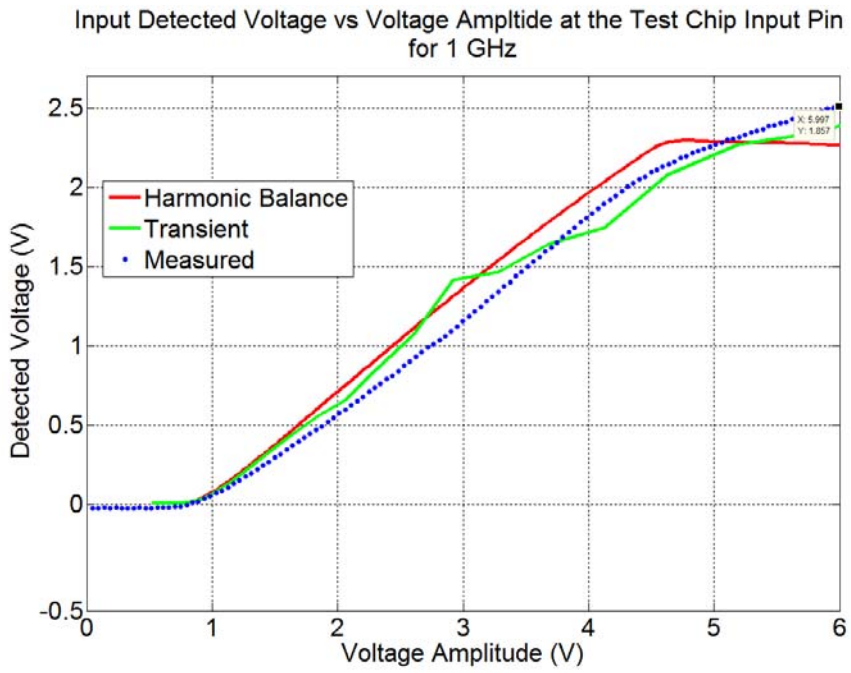

Figure 6.6: Detected voltage predicted by simulation with the body resistor ESD model vs. experiment for input frequency of 1 GHz

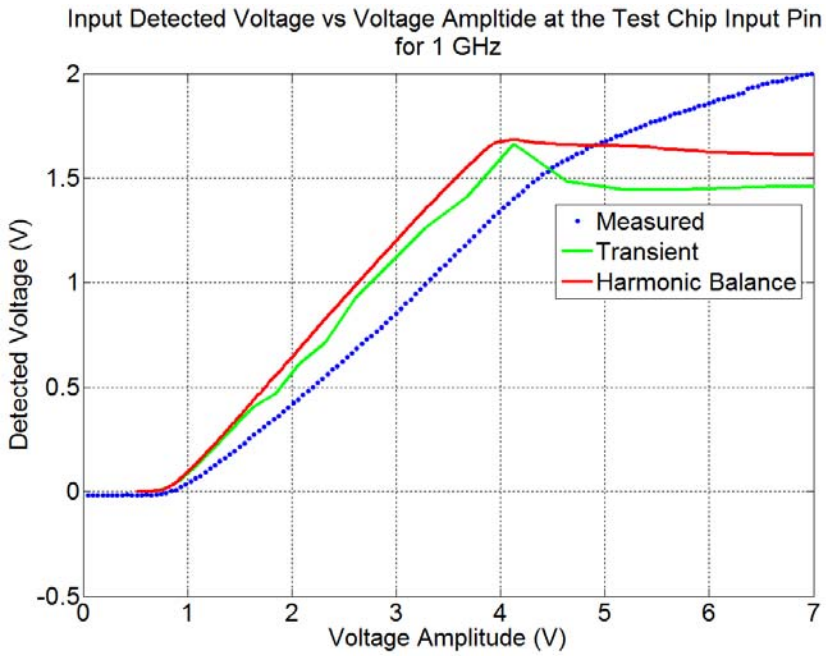

Figure 6.7: Detected voltage predicted by simulation without the body resistor ESD model vs. experiment for input frequency of 2.5 GHz

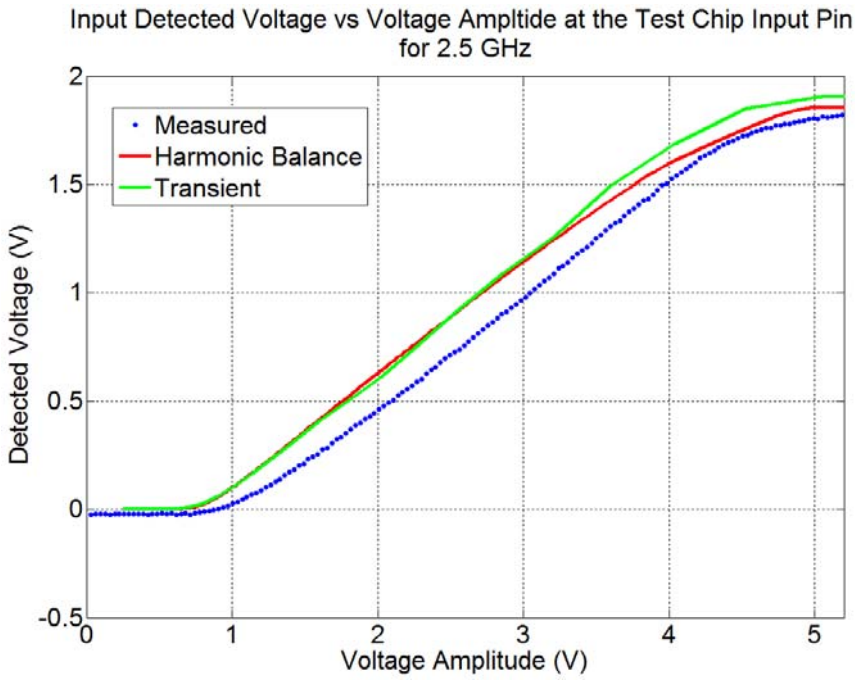

Figure 6.8: Detected voltage predicted by simulation with the body resistor ESD model vs. experiment for input frequency of 2.5 GHz

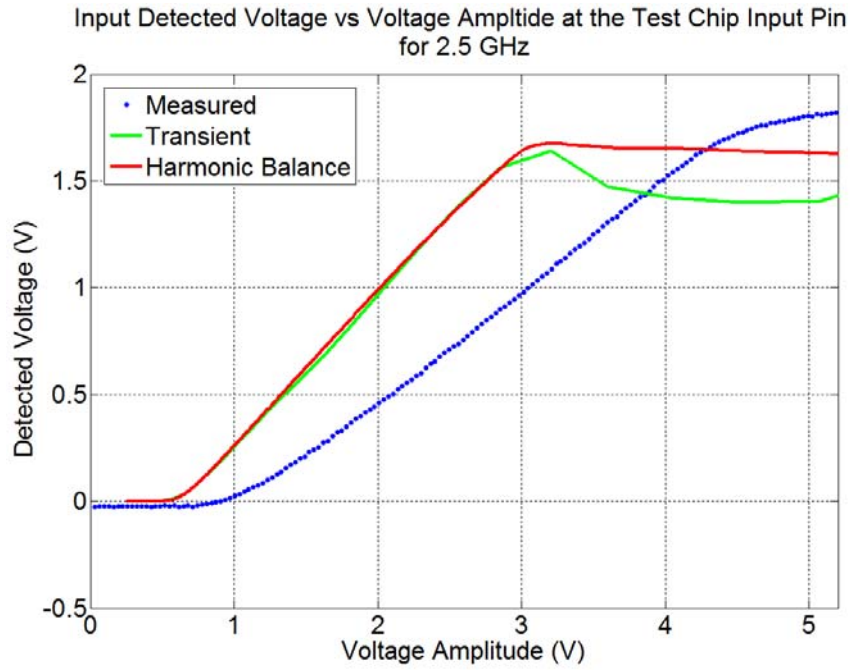

Figure 6.9: Detected voltage predicted by simulation without the body resistor ESD model vs. experiment for input frequency of 2.5 GHz

On the simulation plots where the body resistance model was used, notice the predicted detected voltage shows good agreement with the experimental results, especially for 1 Hz and 2.5 GHz. The simulations which do not use the body resistor model demonstrate the significant improvement the body resistor provides. Notice that the body resistor model also models the imbalance between the detected voltage response of the ggNMOS and the ggPMOS very well. In contrast, the intrinsic BSIM model predicts an even response from both ESD protection devices and the detected voltage levels at 1.5 V for each simulation frequency. Also apparent from the simulation plots is that there is no distinct advantage in terms of accuracy when comparing transient analysis to harmonic balance when evaluating the detected voltage.

6.3 Modeling the Single Inverter Test Circuit

This section presents the results of the modeling technique with respect to the single inverter test circuit. Specifically, this section will focus on the accuracy of the simulation technique described above in predicting the current and output voltage behavior of the test circuit as compared to the measurement results in the previous chapter. Figure 6.10 is the general modeling schematic used for simulation results presented in this section.

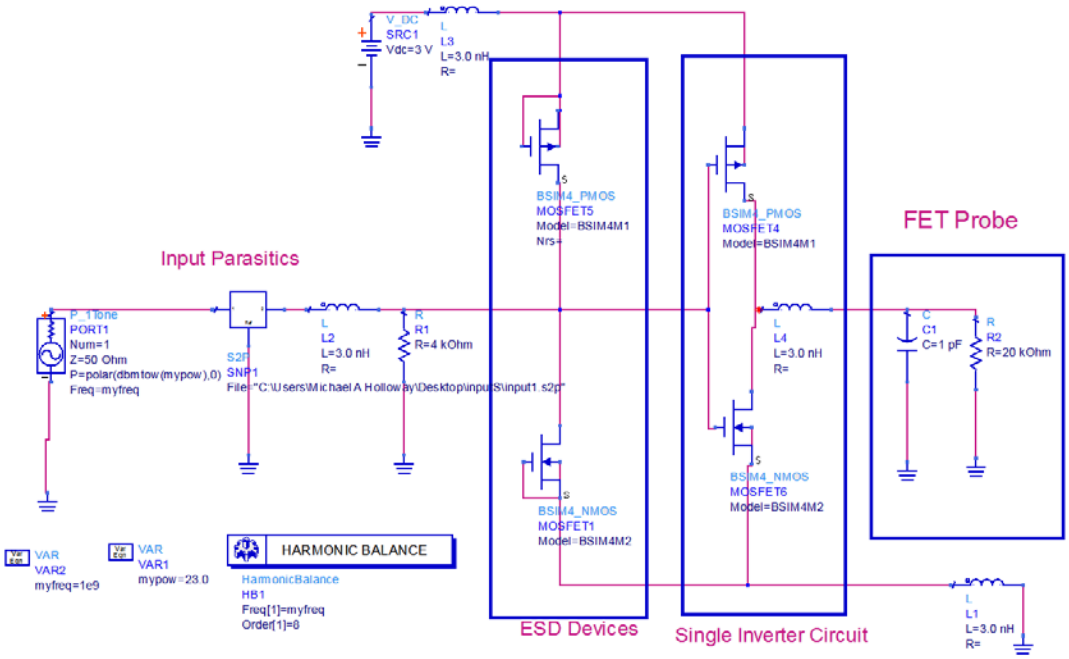

Figure 6.10: ADS Schematic used for single inverter test circuit simulations

An inductance of 3 nH was used to account for the ball-bond wire and lead frame inductances. Since electrical information for the test chip package type is unavailable from the foundry, the value of 3 nH was obtained from [57] and is the average value of the ball bond wire inductance for a similar chip carrier package. The output impedance in the schematic represents the load due to the FET probe used in the measurement experiments.

6.3.1 In-Band Simulation

At in-band frequencies frequencies the ESD protection devices operate in the quasi-static regime for which the basic BSIM junction model is sufficiently accurate. Figures 6.11 shows as a qualitative example the simulation results for an input amplitude of 4 and a frequency 200 MHz.

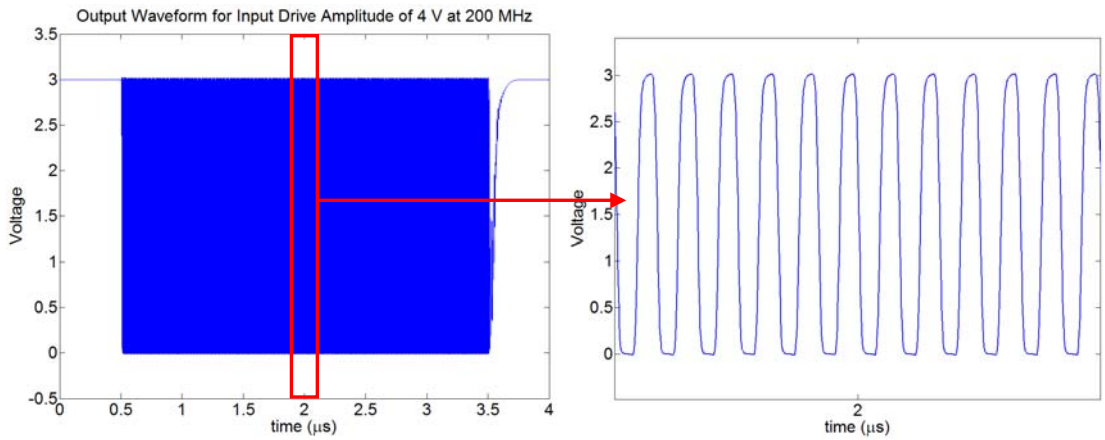

Figure 6.11: Simulation output waveforms for input amplitude of 4 V at 200 MHz for single inverter test circuit.

The simulations results demonstrate similar circuit response to the experimental results shown in figure 5.4. As the input amplitude exceeds the rail voltage the waveform is distorted by the diode action of the ESD devices and produces a signal similar to a normal digital drive waveform at the input. To make the full comparison between simulation and experiment over all drive amplitudes, examine the plots in figure 6.12. The mean value of the voltage and current are plotted for both simulation and experiment.

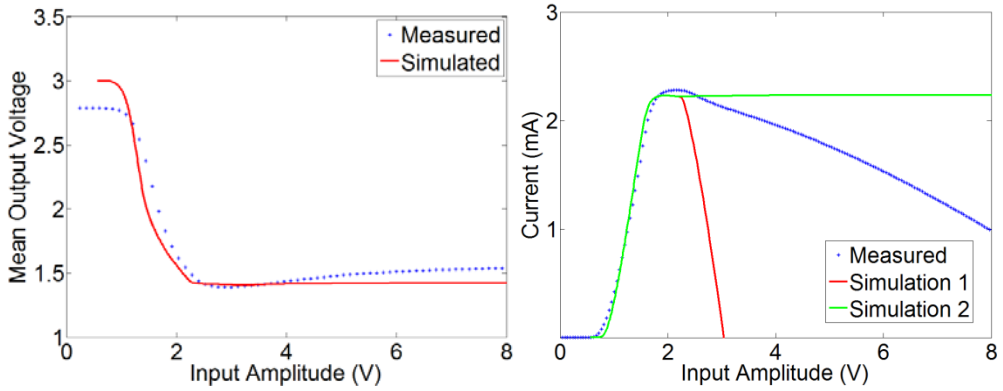

Figure 6.12: Comparison with experiment of the mean output voltage and average current predicted by simulation for the single inverter test circuit with an input frequency of 200 MHz.

There are two important features to clarify in these plots. The first feature is that the simulation current value drops rapidly after the input amplitude surpasses V_{dd}. This is due to the RF current feeding through the ggPMOS while it is forward biased. The power source in the model is an ideal voltage source and hence is a short to ground. In the experiment the RF return path is mostly through the local by-pass capacitor and therefore much less of the RF current is measured by the picoameter. For comparison purposes, the green trace on the top right plot is the current measured from simulation in between the PMOS and the NMOS of the single inverter, which isolates that branch from any of the RF feed through current.

The second feature is the decline in the average DC voltage as after the plateau of 1.5 V is reached. The slump in the voltage level in the experimental measurement is a result of increased distortion of the output waveform. As the input amplitude increases beyond V_{dd}, the voltage fluctuations due parasitic inductance of the ball bond wire and traces add to the output waveform. Figure 6.13 shows the output waveform from the experimental measurement of the test circuit with an input drive of 5.5 V.

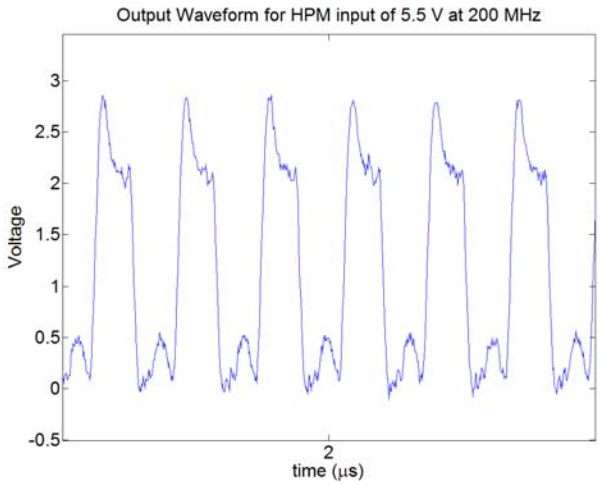

Figure 6.13: Example of output voltage waveform distorted due to overdriven input amplitude

The plot shows that the waveform sharpens at the peak and thus lowers the mean voltage. As the input becomes more overdriven the distortion increases. The simulation plot does not predict distortions of the output waveform as substantial as what was measured in the experiment. This is due to the inadequate modeling of the RF return path through the parasitic of the power rail.

Aside from the variations described above the simulations show good agreement in the context of predicting the threshold of effect. Simulation at low frequencies, in general, is not taxing to the semiconductor analytical models. Quasi-static models will generally perform well and board and trace parasitic impedances do not drastically alter the circuit response in terms of the HPM effects. However it is very important to note, for more advanced technologies in-band may be in the GHz regime. Such is the case of current PC motherboards whose front end busses operate above 1 GHz. When dealing with more advanced technologies parasitic elements must be carefully modeled.

6.3.2 Out-of-Band Simulation

This section presents the results of modeling circuit performance when the input is excite by out-of-band HPM frequencies. At these frequencies experimental results showed that the ESD protection devices will be operating in the NQS regime and parasitic elements have greater influence on effects thresholds. Figure 6.14 is the simulated output waveforms of the single inverter with an input frequency of 1 GHz and amplitude of 4 V. Similar to the results in the experimental plots in figures 5.4 and 5.5, the drive frequency of the input is beyond the switching speed of the circuit, and the output amplitude diminishes compared to in-band frequencies.

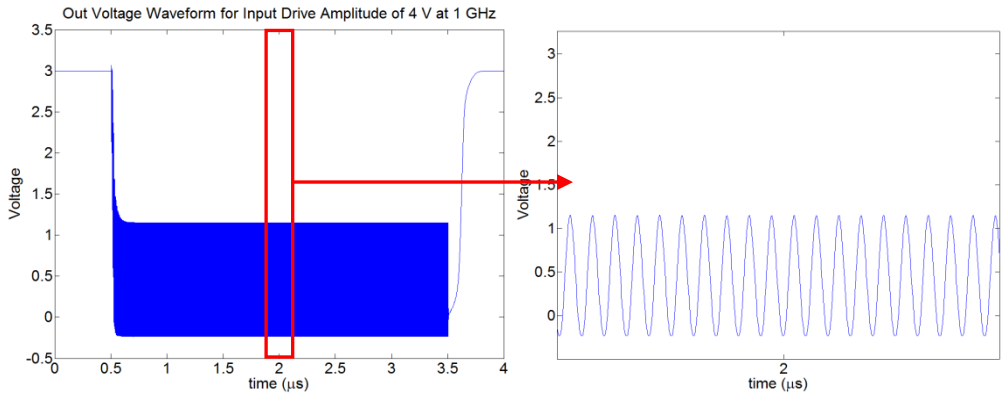

Figure 6.14: Simulation output waveforms for input amplitude of 4 V at 1 GHz for the single inverter test circuit.

To demonstrate the level agreement between the measured circuit response from experiment and the response predicted by simulation the results at 1 GHz and 2.5 GHz are examined. The results from chapter 4 showed significant input response to these frequencies compared to other frequencies across the test bandwidth. The experimental and simulated mean output voltage and average current are plotted for both frequencies in figures 6.15 and 6.16.

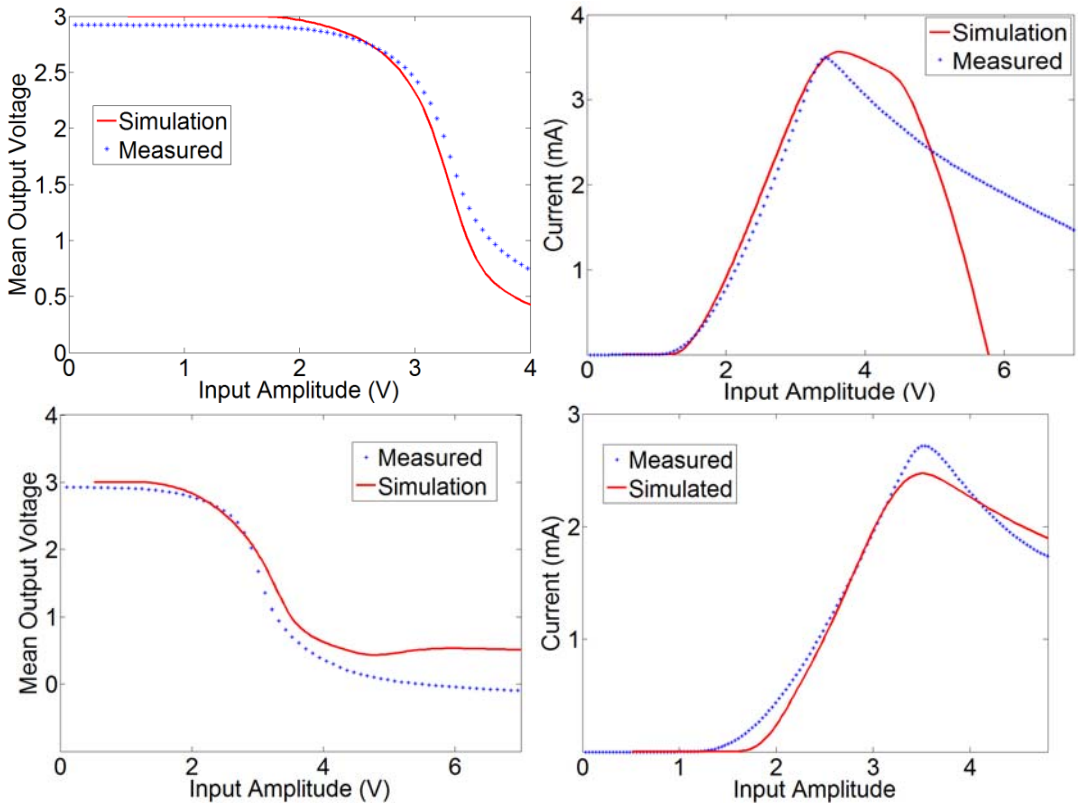

Figure 6.15: Comparison with experiment of the mean output voltage and average current predicted by simulation for the single inverter test circuit for frequencies 1 GHz (top) and 2.5 GHz (bottom).

6.4 Modeling HPM Effects in the CMOS Test Circuits

Chapter 5 presented some very interesting dynamics that occur in IC as a result of HPM interference and the provided evidence that helped determine the cause of these effects. This section presents the modeling of the full test IC's that are representations of basic commercial CMOS IC's. The previous sections demonstrated the accuracy of a modeling technique on simple CMOS devices. The following sections will show how well the modeling techniques handle far more complex circuits with transistors counts that exceed 200. The first half of this section will present in-band effects modeling and the second half will focus on the out-of- band effects.

6.4.1 In Band Effects Modeling on Full test IC's

Results from the previous sections have suggested that at low frequencies, where the quasi-static approximation is valid for the ESD protection circuits, that model predicts circuit behavior very well. Consider the time domain plots of the output voltage for each of the test circuits shown in figure 6.16. Each circuit model was driven at an in-band frequency with an amplitude that exceeded the rail voltage.

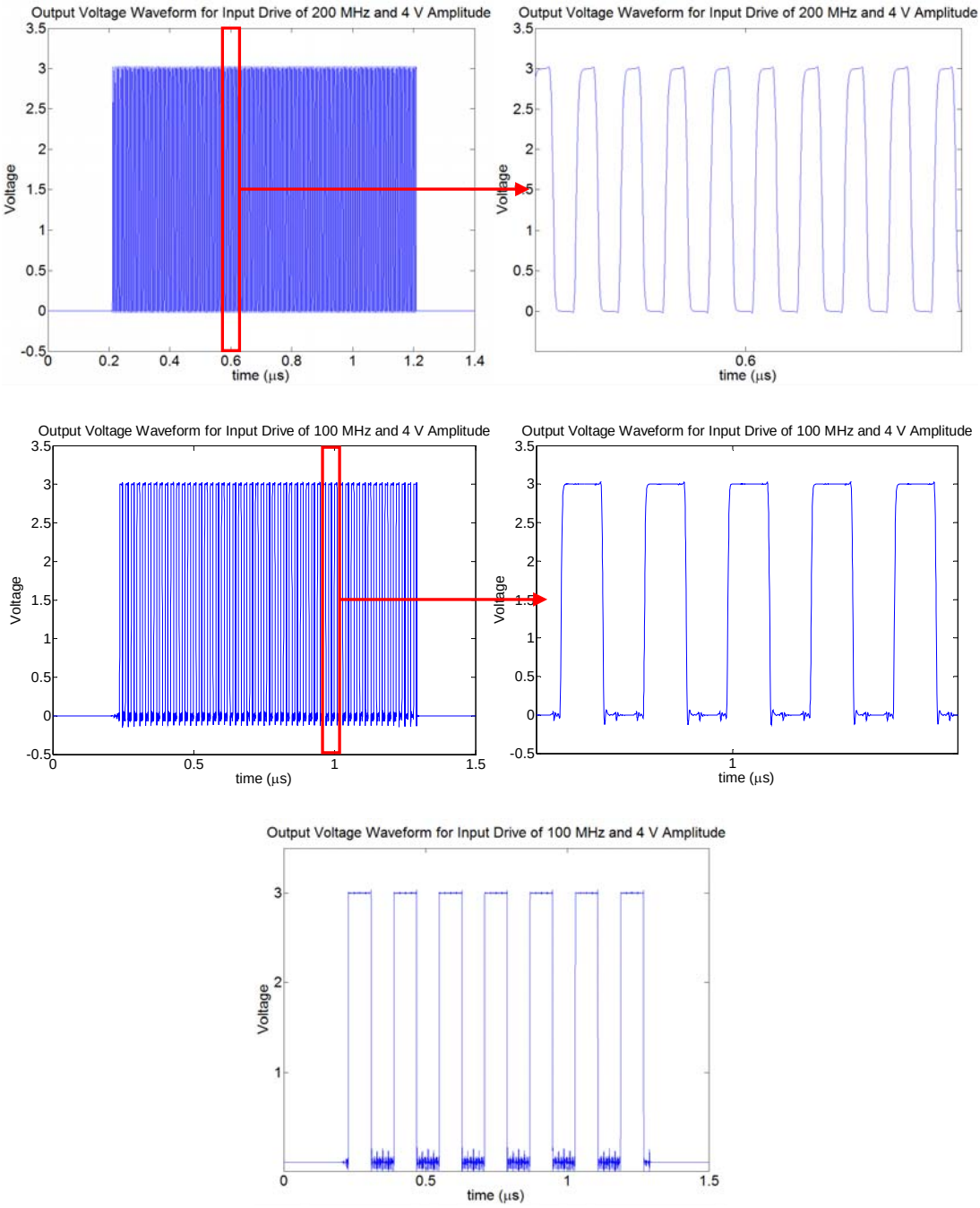

Figure 6.16: Simulation time domain waveforms of the output voltage of the inverter chain circuit (top), JK flip flop (middle), and the most significant bit of the 4 bit counter (bottom)

As was the case with the simple input buffer circuits, the model performs well and predicts the basic behavior of the circuits as described in the previous chapter. Figure 6.17 are plots that compare the mean output voltage and average current as

measured from experiment to the voltage and current predicted by the model over the full test range of input amplitudes.

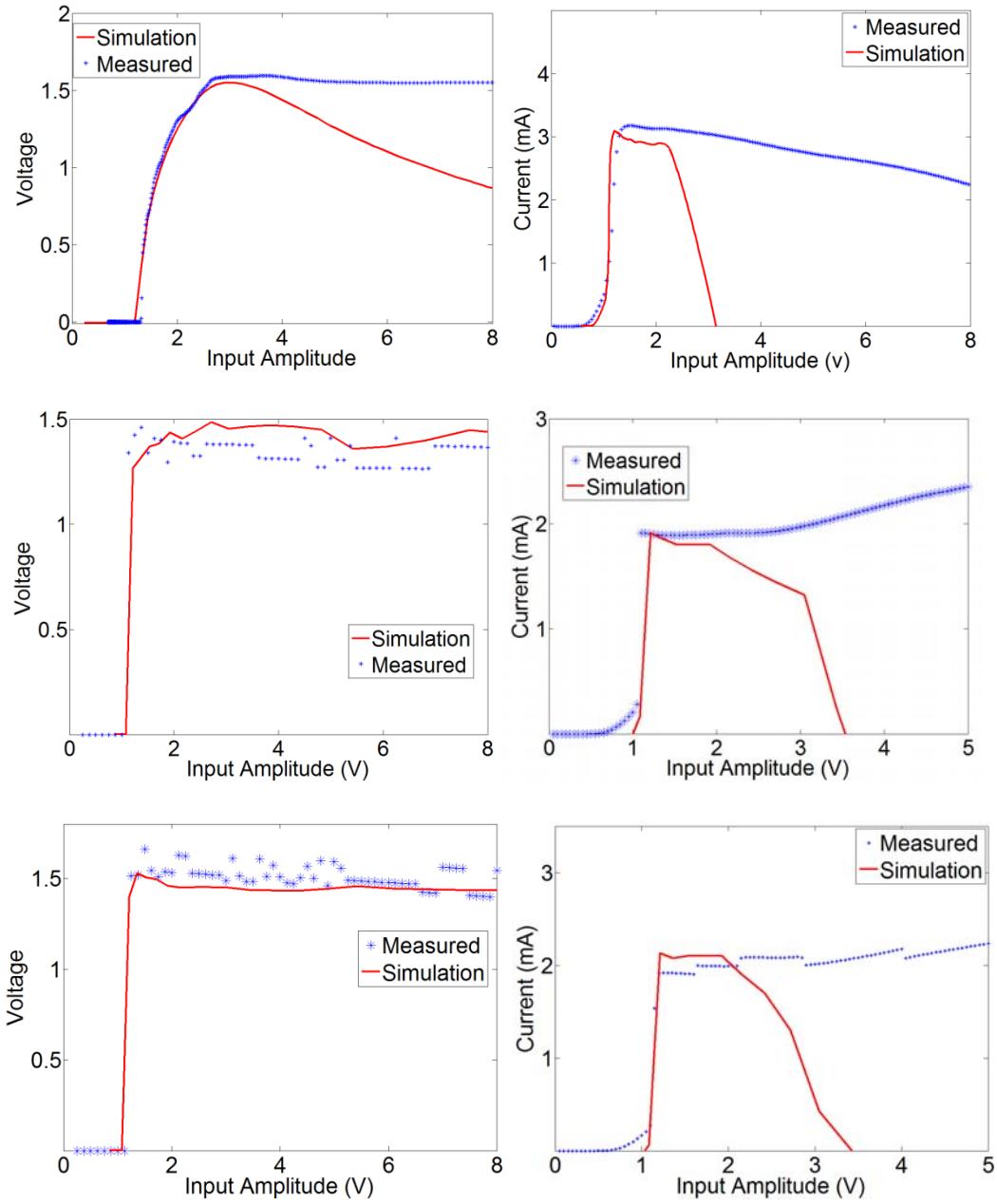

Figure 6.17: Comparison with experiment of the mean output voltage and average current predicted by simulation for the inverter chain circuit at 200 MHz input frequency (top), and the JK flip flop (middle) and 4 bit counter (bottom) with an input frequency of 100 MHz.

The output voltage for the four bit counter in these plots and rest of the plots in this chapter are from the most significant bit.

The model does an excellent job predicting effects thresholds and circuit behavior at these frequencies with the exception if the slump in the average voltage present in the inverter chain circuit. The sag in the voltage is due the same output waveform distortion described in section 6.3.1. The current measurements show the same behavior described earlier in the chapter where the RF feed through current is shorted through the ideal power supply. However, the onset of HPM induced current draw and the peak current value are modeled remarkable well.

6.4.2 Out-of-Band Effects Modeling on Full test IC's

High frequency large signal excitation of commercial IC's have shown to produce the complex circuit dynamics [38]. Modeling these dynamics is a substantial challenge due to the nonlinear device behavior and increase contribution from linear parasitic elements. This section presents the results of the modeling techniques on the CMOS test circuit for HPM signals with out-of-band frequencies. Results will be presented to show where the modeling technique performs very well and where model can be improved and by what means.

In the previous chapter, the output response of the test circuit when under HPM excitation responded in one of two ways for out-of-band frequencies. The HPM either induced a single prompt state change, or the HPM excited nonlinear dynamics through a feedback mechanism, which resulted in phase-locked sub-harmonic output voltage oscillations or aperiodic output voltage oscillations.

Figure 6.18 are the plots of simulation vs experiment for 2.5 GHz input excitation for each of the three test circuits.

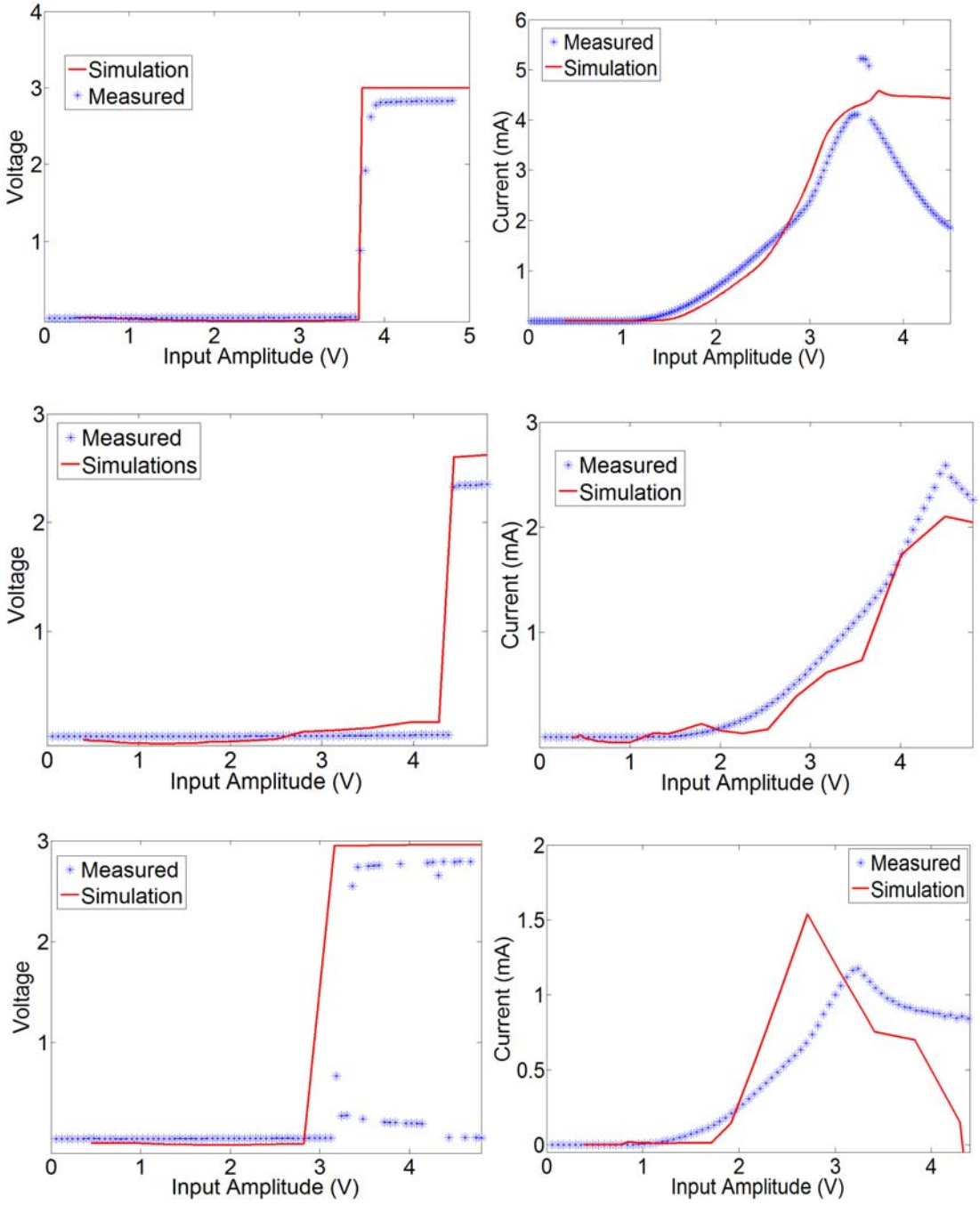

Figure 6.18: Comparison with experiment of the mean output voltage and average current predicted by simulation for the inverter chain circuit (top), the JK flip flop (middle) and 4 bit counter (bottom) with 2.5 GHz input frequency.

Recall that for input HPM frequency of 2.5 GHz, all of the test circuits displayed single bit errors once as the input amplitude increased. For this situation, the model performs very well and does an excellent job of predicting the effect threshold.

The model has more difficulty in predicting the circuit behavior for instances when the nonlinear dynamics occur. First, consider the inverter chain circuit with a 1 GHz drive. The experimental measurements demonstrated sub-harmonic oscillations occurring when the input amplitude reached a value of 5 V. Simulation, however, does not predict these oscillations. Instead, the model predicts a prompt state change similar to the effects observed at 2.5 GHz. The plot of the mean output voltage vs input drive is shown for both experiment and simulation is shown in figure 6.19. The bars on the experimental trace represent the range of output voltages for each input amplitude to better visualize the threshold of oscillations. The mean value is indicated by the marker. The results of the simulation indicate that the model is a very good predictor for the onset of effect but, in this case, does not accurately model the specifics of the output voltage behavior.

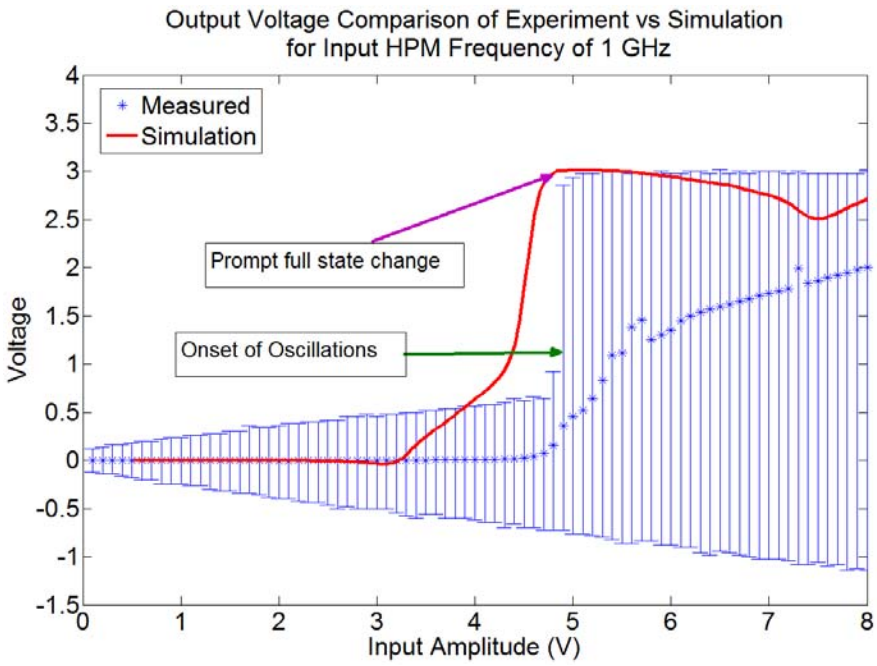

Figure 6.19: Simulation vs. experiment for the output voltage of the inverter chain circuit when driven by a 1 GHz HPM signal

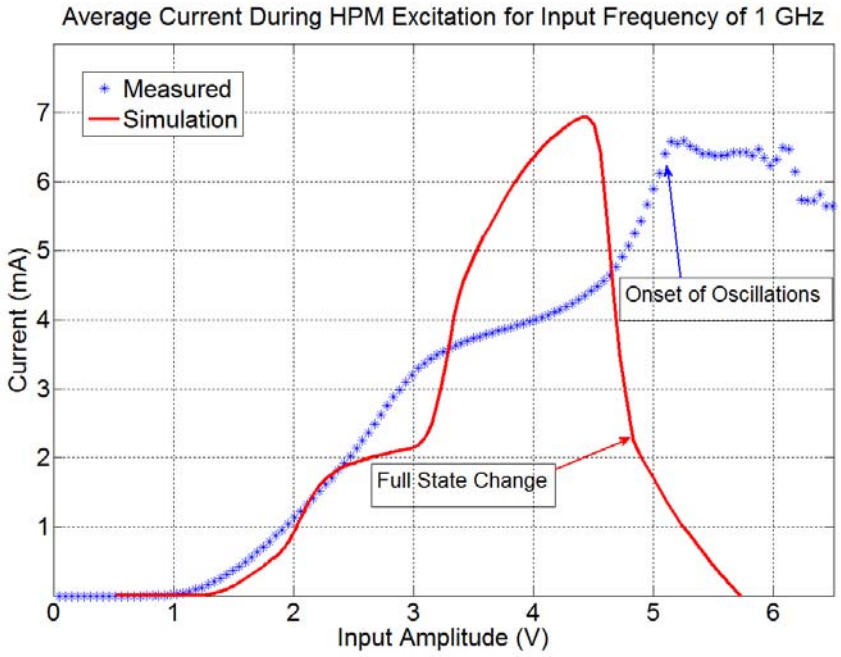

Figure 6.20: Simulation vs. experiment for the average current of inverter chain circuit when driven by a 1 GHz HPM signal

The average current in the simulation demonstrates a similar level of disagreement corresponding to the output voltage behavior. The measured average current value versus measured average current value is plotted in figure 6.20. Notice that the simulation curve looks similar to a drive curve leading up the threshold of the state change in the output voltage. This current behavior is consistent with the similar single bit error effect observed in experiment at 2.5 GHz.

Figures 6.21 and 6.22 are plots of the simulation results for the JK flip flop with input frequency of 1 GHz. The bars in the plot also indicate the output voltage range for each input amplitude as was done in Figure 6.20. Immediately noticeable is the fact that for this circuit, the simulations predict oscillations similar to the ones observed from the experimental results. The prediction for the threshold of effect is within approximately 10% of the measured threshold.

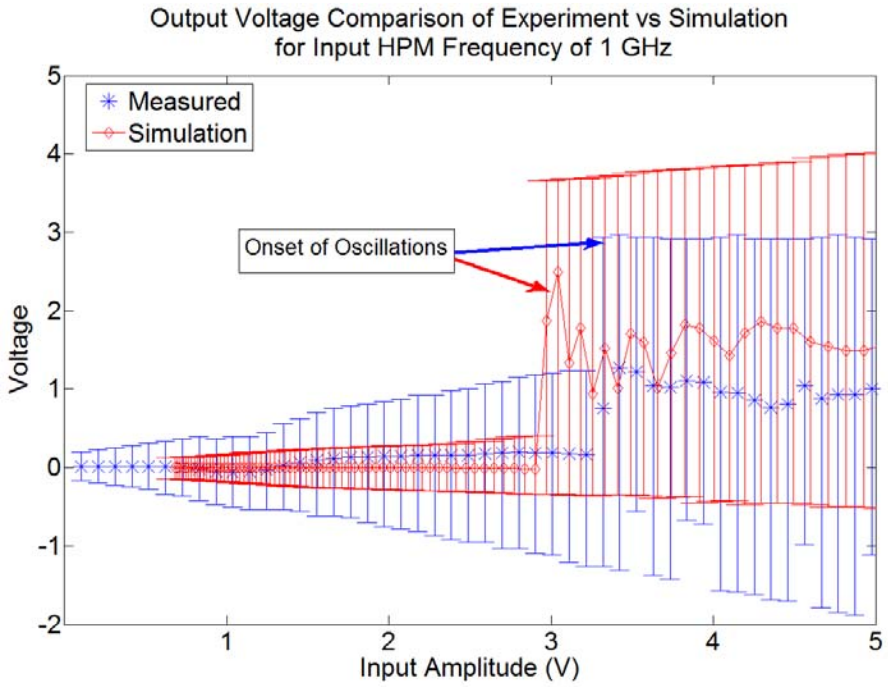

Figure 6.21: Simulation vs. experiment for the output voltage of the JK flip flop circuit when driven by a 1 GHz HPM signal

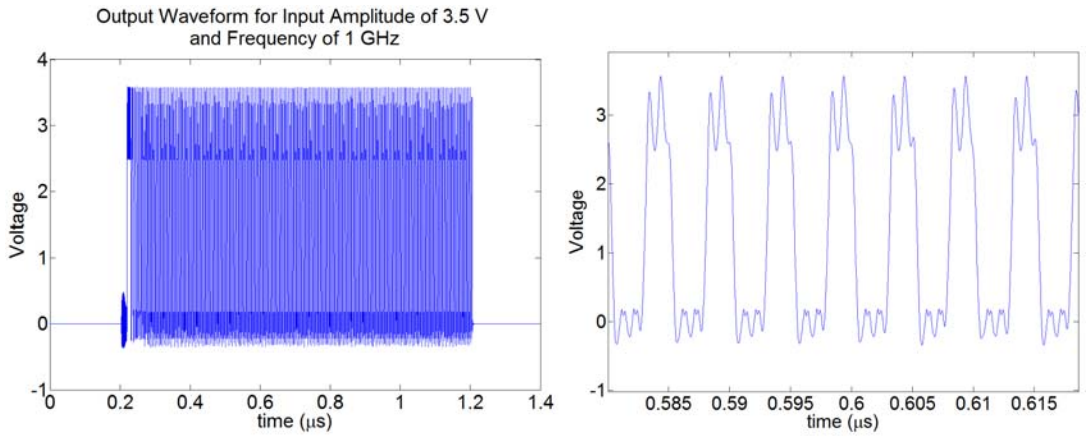

Figure 6.22: Time domain plot of the output voltage of the JK flip flop for an input amplitude of 3.5 V and frequency of 1 GHz

Figure 6.22 is a plot of the output voltage waveform acquired from transient simulation of the JK flip flop circuit for input amplitude of 3.5 V. For the JK flip flop, the simulation predicts that same phase-locking phenomenon that was observed in the experimental measurements at the same frequency. However, the frequency of the oscillation is much higher in the simulation than the experiment. For the situation shown in figure 6.23, the output waveform is only the 3rd sub-harmonic of the drive frequency compared to the 29th sub-harmonic observed in the experiment.

The higher frequency of the output oscillation suggests that the resonant frequency of the feedback in the simulation is larger than the resonant frequency of real feedback path on the test circuit, resulting in a much higher difference frequency. For example, for the inverter chain the oscillation frequency was 34.4 MHz, which suggest that the resonant frequency was the input frequency plus or minus 34.4 MHz (e.g. 1034 GHz). The oscillation frequency of the output for the simulation shown in figure 6.22 is 166.67 MHz, which means the difference frequency is 333.33 MHz since the flip flop divides frequency by 2.

The most likely explanation for the difference in feedback resonance is due to the lack of a robust diffusion capacitance model available in BSIM as was discussed in section 6.2.1. At large amplitudes where the drain body junction of ggPMOS spends more time forward biased, the average excess minority carrier increases resulting in a substantial diffusion capacitance as discussed in Chapter 4. The diffusion capacitance increases exponentially with forward bias as excess minority carriers flood either side of the junction. In order to account for this capacitance accurately, the minority carrier concentration must be modeled well, which includes time dependencies for NQS operation.

Another element that could be improved is the modeling of the linear parasitic elements contained in the V_{dd} traces of the printed circuit board. This involves modeling the RF return path through the small trace and the bypass capacitance to ground. The impedance of the return path likely contributes to the resonance of the feedback. In the simulation model, only the ball bond wire impedance is accounted for in the form of a lumped element inductance. For high frequencies, board trace elements are transmission lines, and cannot be accurately modeled as lumped elements since the impedance could be capacitive or inductive depending on the frequency. Accuracy could be improved by incorporating an S-parameter block similar to the method used for the input parasitic elements.

Simulations of the 4 bit counter also exhibit a similar level of agreement to experiment as the JK flip flop. Figure 6.23 is a plot of the output voltage vs. input amplitude of the 4 bit counter circuit from both simulation and experiment.

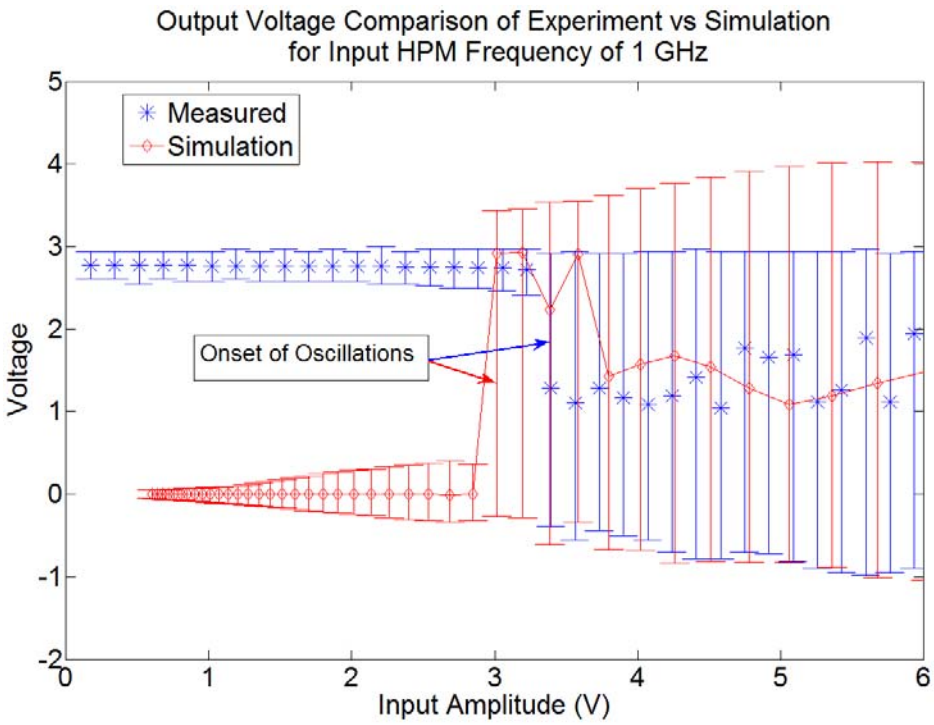

Figure 6.23: Simulation vs. experiment for the output voltage of the most significant bit of the 4 bit counter circuit when driven by a 1 GHz HPM signal

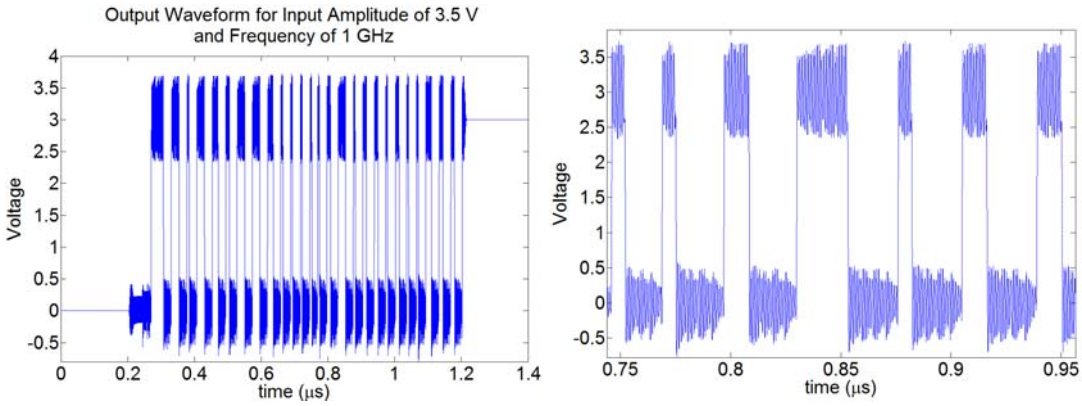

Figure 6.24: Time domain plot of the output voltage of the most significant bit of the 4 bit counter for input amplitude of 3.5 V and frequency of 1 GHz

The voltage output in the plot is from the most significant bit of the counter circuit. The initial output state of the last bit of the counter was high during the experimental measurements. Just as was the case with the JK flip flop, the simulation predicts the

onset of effect within approximately 10% of the actual onset observed in experiment. Figure 6.24 is a simulation plot of the voltage waveform seen at the output of the most significant bit of the 4 bit counter. The simulation was conducted for fixed amplitude of 3.5 V and frequency of 1 GHz. The output voltage oscillations in the simulations also behave aperiodically similar to what was observed in the experiments.

The current plots of simulations and experiment for the flip flop and the counter are presented in figures 6.25 and 6.26. The current measurements for both circuits also show good agreement. The flip flop simulation predicts a peak current about 1 mA lower then was measured but the both simulations predict well the drive amplitude for the onset of HPM induced current draw.

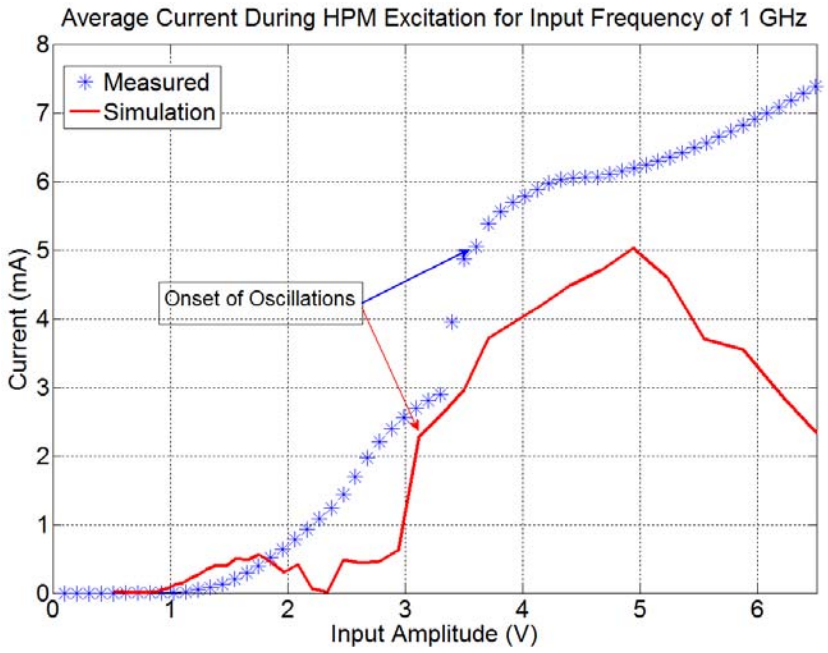

Figure 6.25: Simulation vs. experiment for the average current of the JK flip flop circuit when driven by a 1 GHz HPM signal

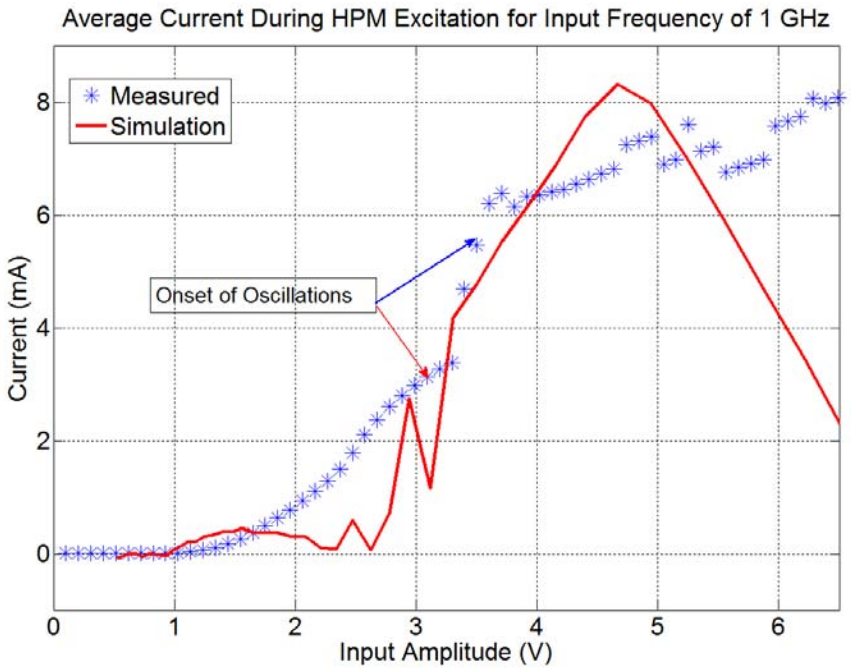

Figure 6.26: Simulation vs. experiment for the average current of the 4 bit counter circuit when driven by a 1 GHz HPM signal

The modeling method predicts the complex effects observed in chapter 5 very well. It should be noted that no oscillations are observed in absence of the ESD protection devices as a whole, the body resistor network, or the parasitic inductances elements, which further supports the hypothesis that the resonant feedback path though the V_{dd} line and the ESD protections circuits.

Since the circuit simulator is capable of reproducing the complex dynamics observed in experiment, simulations can be used to further study the dynamics and confirm the hypothesis presented Chapter 5. Consider the schematic in Figure 6.27. The model consists of The JK flip flop without the ball bond wire inductance present at the device power pin. The DC power supply is replaced with an ideal AC sinusoidal voltage source.

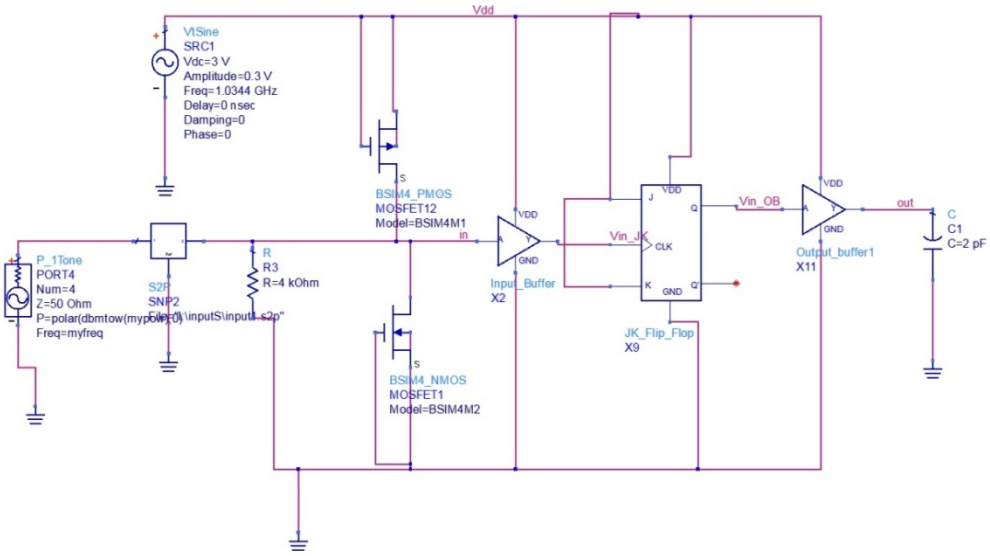

Figure 6.27: Schematic used for simulation verification of oscillation dynamics.

The AC source is given a DC offset of 3 V to set the rail voltage and the AC frequency is set to 1.034 GHz with amplitude of 0.3 V in to imitate the feedback resonance observed in the experiments. The input signal is the same as the previous simulations with the power set to produce an amplitude of 3.5 V at the device terminal. The results of the simulation are shown in Figure 6.28.

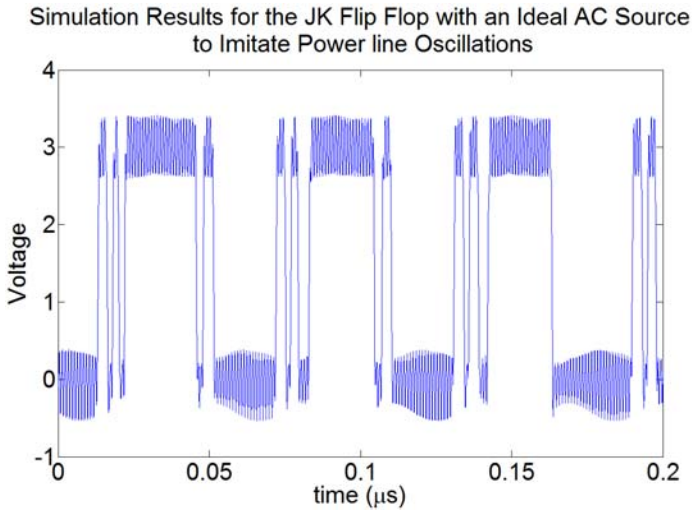

Figure 6.28: Output voltage results of the simulation of the JK flip flop circuit in Figure 6.27.

The period of the output waveform is approximately 60 ns, which twice the period of difference frequency of 34.4 MHz. In other words the oscillations are being driven by the half difference frequency since the flip flop divides frequency by 2. The results demonstrate the same phase-locking phenomenon observed in experiment and show that the oscillation correspond to the difference frequency. This also confirms that spurious output oscillations can be caused by feedback through the V_{dd} line and the ESD protection circuit.

Chapter 7 : Discussion and Conclusions

The experimental results presented in this dissertation contribute to the greater understanding of HPM effects on CMOS technology at the device and circuit level. Most importantly, this work demonstrated that deterministic methods can be successfully employed to predict the threshold of effect in fundamental circuits based on scalable device parameters. The research presented in this dissertation is part of a foundational to a new approach to the evaluation of system susceptibility, which involves the combined effort of analytical circuit models and statistical determination of port voltages in structures with complex geometries. This chapter concludes the dissertation by highlighting the key results in the experimental and modeling efforts and discussed future work that will contribute to the progress of this promising area of research.

7.1 Summary of Experimental Results

The experimental approach for this work involved the fabrication of the custom CMOS digital circuits. The circuits were design to resemble the structure of basic commercial digital IC's. Custom designed chips offer the advantage of complete knowledge of the circuit and device structures. Experiments on the custom IC's were performed using a method where HPM signals are directly coupled into the test structures. The experimental apparatus was carefully design with intent of precisely determining the terminal voltage at the input and output of the test circuits.

Experimental measurements conducted on the input terminal of the test circuits demonstrated the prominent role of ESD protection devices in HPM effects.

ESD protections devices are ubiquitous circuits that are crucial reliability assets to the microelectronics industry. The results of the experiments on the commonly used ggNMOS and ggPMOS reveal that the large PN junction associated with ESD devices distorts the HPM signal and introduce DC biases to the input of the digital circuit. At high frequencies the PN junction enters the NQS regime when transient response of the junction potential becomes comparable to the period of the HPM signal. Theory predicts and experimental results confirmed that the response of the ggNMOS and ggPMOS is uneven primarily due to the difference in the diffusion of minority carrier, which governs diode transients. The ggNMOS had stronger response at higher frequencies than the ggPMOS, which resulted in detected voltages at the input that approached V_{dd}.

For HPM excitation frequencies within the normal operating range of the circuit, the input signal is rectified and resembles a normal logic waveform, which drives the circuit. Effects of this nature were classified as in-band effects. The output voltage of the circuit resembles the normal response of the circuit to a logic signal and the current behavior is predicted by established theory.

HPM excitation frequencies beyond the normal operation band of the test circuits were classified as out-of-band effects. The results show that out-of-band HPM excitation can produce both single bit errors and spurious oscillations. Single bit errors are the result of input DC biases generated by the ESD protection devices. Due to the imbalance between the response of the ggNMOS and the ggPMOS, the DC increases beyond the switching point of the CMOS devices as the input HPM

amplitude increases. The result is single state change that persists for the duration of the HPM pulse.

The second out-of-band effect observed due to HPM excitation was spurious voltage oscillations at the output of the circuit, with characteristic frequencies much lower than the excitation frequency. Analysis performed in the experimental measurements and simulations conducted chapter 6 support the hypothesis that the oscillations are the result a feedback mechanism. The feedback path is likely through the Vdd line and the ggNMOS ESD protection to the input of the circuit. The frequency of the feedback resonance and the fundamental frequency mix due to circuit nonlinearities to produce a difference frequency, which modulates the V_{dd} voltage oscillations. The fluctuation of the Vdd power periodically creates a condition where the input HPM signal will induce a state change in the circuit. In some cases the difference frequency is near a sub-harmonic of the input signal and the output oscillations phase-lock with the input HPM signal. Analysis of experimental results revealed that state changes occur when the phase of the Vdd voltage is $-\pi/2$ the same time the phase of the input is $\pi/2$, indicating the input voltage is at its maximum and the V_{dd} voltage is at its minimum.

The current is composed of a short circuit component and a dynamic component. The deviation from theory occurs because the high frequency fundamental component of the HPM is attenuated by the frequency response of the circuit and the signal does not fully switch the CMOS devices. As a result the contribution of the short circuit component of the total average current increases compared to when the device fully switches as the DC level increases with higher

input amplitudes. In contrast, the dynamic component decreases due to lack of full state switching. The exception to this is the circumstance when spurious output oscillations occur. This effect produced current high current levels, which are produced by DC bias at the input buffer stage and the dynamic current created by the voltage oscillations at the output. It was shown that large devices such as buffer circuits, account for most of the HPM induced average current draw due the dependence of the total current on load capacitances and device geometry.

The experimental results can be used to draw some general conclusions about the susceptibility of CMOS microelectronics. However, these conclusions need to be placed in the proper context. The experimental results presented the effects thresholds in terms of voltage amplitude at the device terminals. In realistic HPM scenarios radiation couples the circuit traces to produce the terminal voltages. The following analysis is an approximation of the radiated power density needed at the printed circuit board surface to produce the necessary terminal voltage to excite HPM effects.

For this analysis, a printed circuit board trace of length 3 cm is chosen to represent the radiation coupling aperture. The frequency of the radiation will range from 100 MHz to 2 GHz. The board trace can be approximated as a Hertzian dipole since the wavelengths range from 3 m to 15 cm. The average power radiated by a Hertzian Dipole is given by equation 7.1 with the radiation impedance given by equation 7.2 [68].

$$P_{rad} = 80\pi^2 \left(\frac{dl}{\lambda}\right)^2 \frac{\left|\hat{I}\right|}{2} \tag{7.1}$$

$$R_{rad} = 80\pi^2 \left(\frac{dl}{\lambda} \right)^2 \tag{7.2}$$

dl is the dipole length, λ is the wavelength, and $\hat{I}$ is the current amplitude. The current is calculated by using the terminal voltage and the radiation resistance given by equation 7.2. The voltage amplitude for the threshold of effect for each of the test circuits over the frequency band of 100 MHz to 2 GHz ranged from 1.2 V to 5 V. The lower threshold voltages tend to represent the in-band effects while the larger threshold voltages were typical of out-of-band effects. To make a more general approximation this voltage range is used to calculate the power density for each wavelength and thereby making no assumptions about which frequency is in-band or out-of-band for a given circuit.

To estimate how effects threshold scale, this analysis is performed for the TSMC 0.25 μm process and the TSMC 0.13 μm process. For the two more advanced technologies it will be assume that the ESD protection circuit design is roughly the same as the one used in the test circuits. The effects thresholds for each of the TSMC technologies is estimated by assuming that the effects threshold voltages are the same percent of V_{dd} as the ones measured on the AMI 0.6 μm process. V_{dd} used for the TSMC 0.25 μm process and the TSMC 0.13 μm is 2 V and 1.2 V respectively. The voltage is determined by the process information found at [43]. The estimated power density versus frequency is plotted in figure 7.1 for each of the three technologies.

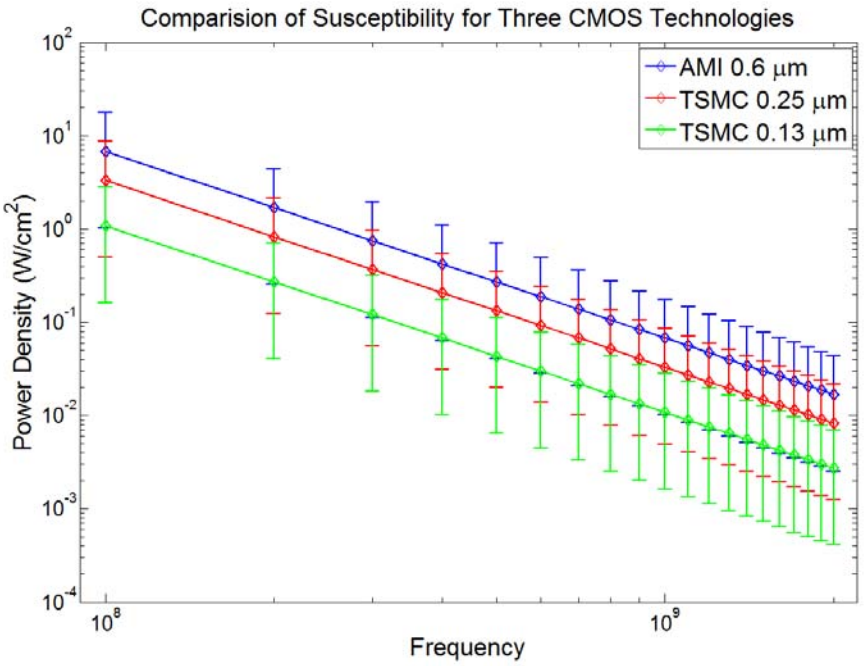

Figure 7.1: Estimation of the radiation power density needed to stimulate HPM effects

The bar lines represent the full range of power density calculated from the effects threshold voltage range relative to each process technology. The higher range of the bars will represent out-of-band thresholds while the lower bars tend to represent in-band threshold. Notice that when considering the radiation coupling, susceptibility increases with frequency, which is the opposite conclusion that would be drawn if one only consider the results of the experiments based purely on the terminal voltages. The reason for this is that as the HPM wavelength approaches the resonant length of the board trace, larger voltages are produced on the traces with lower power densities at the board surface. Essentially, less RF power is required to create larger terminal voltages at higher frequencies.

The results of the analysis can be used to infer some general scaling laws for HPM effects. The plot indicates that the power density needed to produce effects

scales by $1/f^2$. Also, as the gate length is reduced by a factor of two, the power density needed to produce effects is approximately reduced by a factor of three.

7.2 HPM Effects Modeling

The modeling techniques developed in this research utilized the industry standard BSIM analytical device model along with the commercial simulation software Agilent Advance Designed Systems (ADS). A simple but effective technique was used to account for the NQS behavior of the ESD protection devices. This technique involved using a body resistor network, which places a resistance between the drain body PN junction and the source and body contacts. The resistor creates a time constant with the junction capacitance of the drain body diode. The time constant imitates the transition time of the reverse recovery process of the PN junction. Without the time constant the BSIM PN junction model transitions from forward bias to reverse bias almost instantaneously and the models response is very inaccurate at high frequencies. The technique proved to be an efficient and effective means of simulating the NQS behavior of the ESD devices at the input terminal of the HPM test circuits using BSIM compact models. Results of simulations showed that the technique improves accuracy of the HPM effects model substantially across the entire experimental frequency range for both in-band and out-of-band effects threshold prediction. Specifically, the model improves the accuracy of the predicted input ESD response in the NQS regime, and allows for simulation of the conditions that lead to single bit errors and spurious output oscillations. The simulations also incorporated an S-parameter model to account for the impedance of the input trace of the printed circuit board. The S-parameters were derived from a measurement of the

boards trace with a vector network analyzer, and the technique proved highly effective in improving the accuracy of the simulations.

Simulations of the full test circuits proved to an excellent predictor of the threshold of effect when compared to the experimental results. The modeling technique does have some difficulty in reproducing the precise circuit behavior for the more complex dynamics observed at high frequencies. This is primarily due to a lack of accounting for the diffusion capacitance in the diode model inherent in BSIM. Introducing a model that accounts for the diffusion capacitance and the minority carrier transients would do the most to improve overall accuracy of the model. This can be achieved one of two ways. One way would be to incorporate a separate semi-conductor model that has better diode modeling capabilities. To use such a model would require a separate parameter extraction of the ESD devices to acquire the parameters specific to that model. Another approach would be to improve upon BSIM's drain/source to body diode model. This would involve adding to or altering the core analytical expression of BSIM. Ultimately, improving the model will depend on the intent of its use and is a question of expediency versus accuracy.

7.3 Future Work

This work has provided an excellent technique for predicting the threshold of effect in simple digital IC's. The next step in this work is to begin testing the combination of statistical techniques for evaluating field distributions in complex structures with deterministic circuit models. The experimental approach involves using a microwave source to illuminate a target microelectronic device. Test boards

have already been design and fabricated for these experiment and an example is shown in figure 7.2.

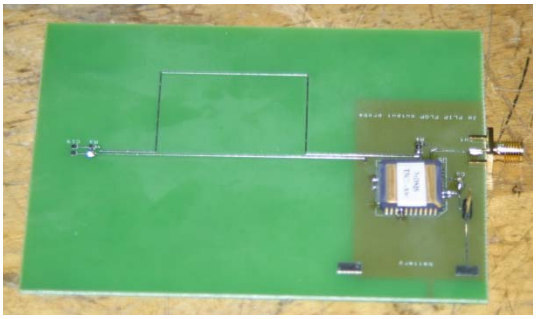

Figure 7.2: Example device build for RF illumination experiment

The input trace of the board is specifically designed to encourage EM coupling to the circuit to reduce power demands on the microwave source. The input trace's radiation impedance will be used as the "port" impedance need for the Random Coupling Model mentioned in Chapter 1. The RCM will be used to predict the probability density of the terminal voltages at the device input. The modeling technique developed in the research presented in this dissertation will be used to determine the effects threshold. That information can then be used to integrate the voltage PDF and predict the probability of effect.

A special anechoic chamber was constructed to perform measurements to validate probability of effect calculations derived from RCM calculations and circuit modeling. Figure 7.3 is a photograph of the chamber.

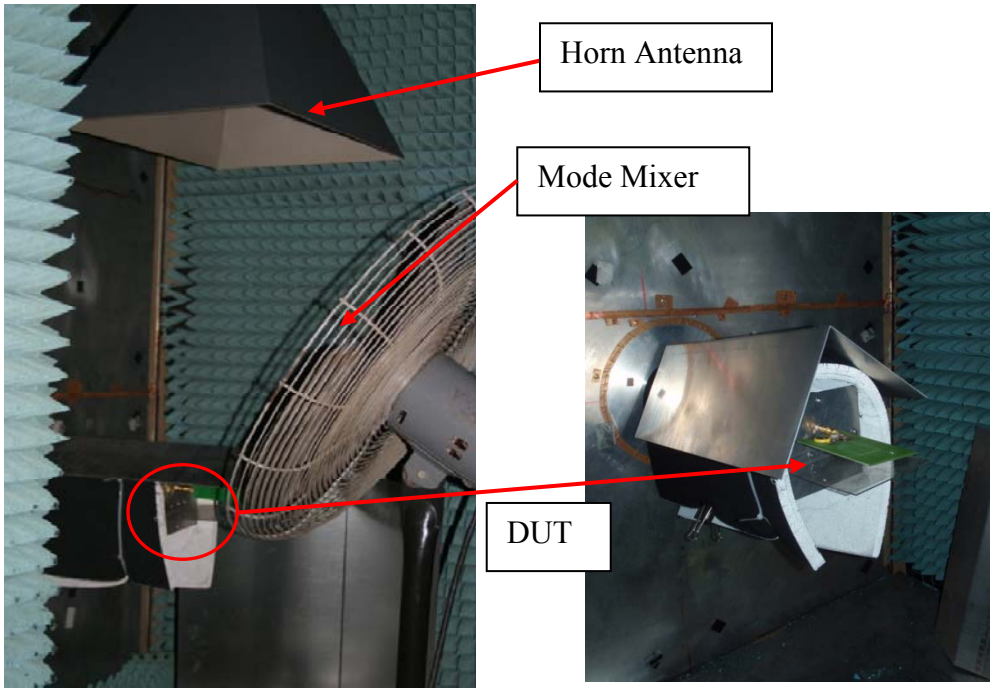

Figure 7.3: Anechoic chamber designed for HPM effects testing

The chamber is designed with removable absorber panels on the sidewalls so that the resonant characteristic of the chamber can be varied. This capability also allows the chamber to be configured with irregular boundary conditions, which is important for imitating more realistic complex enclosures such as aircraft cockpits. The device under test is connected to instrumentation through a shielded arm that extends into the chamber.

Another import area of future work is the development of effective HPM counter-measures. Any system that communicates with the outside world has a way for HPM to couple into to electrons. Heavy shielding may not practical for many civil systems and other more advanced techniques need to be developed to improve system immunity to HPM effects. Some approaches to mitigation include designing new ESD structures to reduce their influence on HPM effects, opto-isolation of device

pins using single photon detectors and low power diodes, and using low voltage differential signaling (LVDS) between critical communication nodes.

Some initial work on evaluating how well LVDS reduces HPM susceptibility has already begun. LVDS signals are transmitted differentially and utilize the high common mode rejection of differential amplifiers to reduce noise. This type of signally is not normally used for typical circuit boards traces. The concept is that this form of circuit board signally may reduce the level of the RF that enters the circuit since RF will be common on both of the differential signal lines. Custom LVDS circuits were designed and fabricated, and initial test evaluations were performed using the modeling techniques presented in this study. Initial results show that this signaling technique may be very effective in reducing susceptibility.

7.4 Closing Remarks

There is no doubt that HPM effects evaluation is a complex and difficult problem. The challenge of evaluating more complex systems awaits and the separation point where deterministic methods are practical and statistical method are needed is likely to be less clear as the systems become more complex. The foundational work present in this dissertation provides an essential element to the task of building accurate and comprehensive evaluation techniques necessary for HPM threat assessment. For the first time an accurate method of determining HPM effects based on scalable device parameters has been demonstrated. The method presented here can be incorporated into the design cycle to determine susceptibility levels and evaluate counter measures effectiveness. The analysis of the experimental work provides detailed explanations for many of the effects observed in previous

experiments conducted on commercial devices, which to date have never been fully characterized. The fundamental knowledge of HPM effects provided by the research in this dissertation can be use formulate new strategies to deter the threat of HPM and facilitate the design of more robust HPM counter-measures.

Appendix: BSIM Parameters

NMOS Paramters:

```
MODEL CMOSN NMOS LEVEL   = 49
+VERSION = 3.1       TNOM = 27           TOX = 1.39E-8
+XJ = 1.5E-7         NCH = 1.7E17        VTH0 = 0.6608467
+K1 = 0.882934       K2 = -0.1000983     K3 = 26.2438717
+K3B = -8.6915991    W0 = 1.05011E-8     NLX = 1E-9
+DVT0W = 0           DVT1W = 0           DVT2W = 0
+DVT0= 0.7528463     DVT1 = 0.3513026    DVT2 = -0.5
+U0 = 452.2603392    UA = 1E-13          UB = 1.267483E-18
+UC = -1.07249E-13   VSAT = 1.918393E5   A0 = 0.7538792
+AGS = 0.1477745     B0 = 1.812342E-6    B1 = 5E-6
+KETA = -3.52756E-3  A1 = 1.724085E-6    A2 = 0.3
+RDSW = 992.3287671  PRWG = 0.1314454    PRWB = 0.0147472
+WR = 1              WINT = 2.33239E-7   LINT = 7.874629E-8
+XL = 1E-7           XW = 0              DWG = -8.015118E-9
+DWB = 4.481996E-8   VOFF = -1.14742E-4  NFACTOR = 1.1118905
+CIT = 0            CDSC = 2.4E-4       CDSCD = 0
+CDSCB = 0          ETA0 = 6.720698E-3  ETAB = 0.3926806
+DSUB = 0.2349451   PCLM = 1            PDIBLC1 = 7.070387E-3
+PDIBLC2 = 0.020295 PDIBLCB = 0.5       DROUT = 0.5
+PSCBE1  = 5.57029E8 PSCBE2  = 3.0023E-4 PVAG = 0.0205112
+DELTA = 0.01       RSH = 87.5          MOBMOD  = 1
+PRT = 0            UTE = -1.5          KT1 = -0.11
+KT1L = 0           KT2 = 0.022         UA1 = 4.31E-9
+UB1 = -7.61E-18    UC1 = -5.6E-11      AT = 3.3E4
+WL = 0             WLN = 1             WW = 0
+WWN = 1            WWL = 0             LL = 0
+LLN = 1            LW = 0              LWN = 1
+LWL = 0            CAPMOD = 2          XPART = 0.5
+CGDO= 1.82E-10     CGSO = 1.82E-10     CGBO = 1E-9
+CJ = 4.148308E-4   PB = 0.8419648      MJ = 0.4306191
+CJSW = 3.47157E-10 PBSW = 0.8          MJSW = 0.1998567
+CJSWG   = 1.64E-10 PBSWG = 0.8         MJSWG = 0.1998567
+CF = 0             PVTH0 = -0.0200252  PRDSW = 500
+PK2 = -0.0709258   WKETA = 2.563816E-3 LKETA = 0.0305584
```

PMOS Parameters:

```
.MODEL CMOSP PMOS LEVEL   = 49
+VERSION = 3.1       TNOM = 27            TOX = 1.39E-8
+XJ = 1.5E-7         NCH = 1.7E17         VTH0 = -0.9152268
+K1 = 0.553472       K2 = 7.871921E-3     K3 = 0.0950177
+K3B = -0.1423064    W0 = 1E-8            NLX = 5.895906E-8
+DVT0W = 0           DVT1W = 0            DVT2W = 0
+DVT0 = 0.6170129    DVT1 = 0.3544724     DVT2 = -0.3
+U0 = 201.3603195    UA = 2.408572E-9     UB = 1E-21
+UC= -1E-10          VSAT = 8.58603E4     A0 = 0.7681699
+AGS = 0.1112568     B0 = 5.442042E-7     B1 = 0
+KETA = -4.86578E-3  A1 = 3.048892E-4     A2 = 0.7243398
+RDSW = 3E3          PRWG = -0.0300686    PRWB = -0.0443405
+WR = 1              WINT = 2.52191E-7    LINT = 1.184165E-7
+XL = 1E-7           XW = 0               DWG = -3.978501E-9
+DWB = -1.09102E-8   VOFF = -0.0747511    NFACTOR = 1.0511576
+CIT = 0             CDSC = 2.4E-4        CDSCD   = 0
+CDSCB = 0           ETA0 = 3.072197E-4   ETAB    = -0.2
+DSUB = 1            PCLM = 2.2700252     PDIBLC1 = 0.0662538
+PDIBLC2 = 3.6467E-3 PDIBLCB = -0.048886  DROUT = 0.2932626
+PSCBE1= 1E8         PSCBE2 = 3.342777E-9 PVAG = 8.381464E-4
+DELTA = 0.01        RSH = 112.1          MOBMOD  = 1
+PRT = 0             UTE = -1.5           KT1 = -0.11
+KT1L = 0            KT2 = 0.022          UA1 = 4.31E-9
+UB1 = -7.61E-18     UC1 = -5.6E-11       AT = 3.3E4
+WL = 0              WLN = 1              WW = 0
+WWN = 1             WWL = 0              LL = 0
+LLN = 1             LW = 0               LWN = 1
+LWL = 0             CAPMOD = 2           XPART = 0.5
+CGDO = 2.21E-10     CGSO = 2.21E-10      CGBO = 1E-9
+CJ = 7.191339E-4    PB = 0.8658375       MJ = 0.4881106
+CJSW = 2.23284E-10  PBSW = 0.8411626     MJSW = 0.1961013
+CJSWG = 6.4E-11     PBSWG = 0.8411626    MJSWG = 0.1961013
+CF = 0              PVTH0 = 5.98016E-3   PRDSW = 14.8598424
+PK2 = 3.73981E-3    WKETA = 0.0149527    LKETA = -0.0137133
```

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